Evolvable Hardware

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Contents of this talk

- Basic Concept of Evolvable Hardware
- Digital Hardware Evolution
  - Gate-level Evolvable Hardware
    - EMG prosthetic hand
    - Autonomous Robot
    - Data compression for electrophotographic printer
  - Function-level Evolvable Hardware
    - Autonomously reconfigurable neural network chip
- Analogue Hardware Evolution
    - Analogue EHW chip for cellular phones
    - EHW-based high speed clock architecture
- Research Trends

Evolvable Hardware (EHW)

Conventional Hardware	Evolvable Hardware
Specification fixed	Spec. changes dynamically
Architecture fixed	Architecture changeable ⇒ Hardware circuit is autonomouly synthesized.

EvolvableHardware =

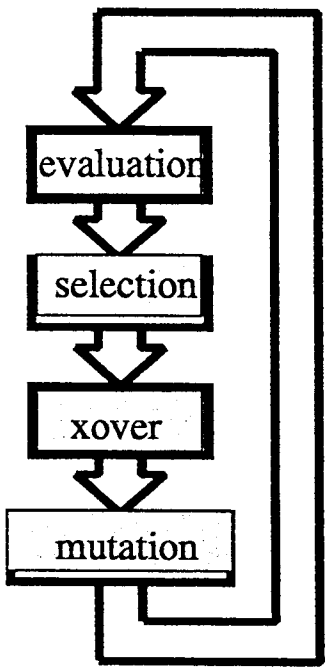
Evolutionary Computation

+

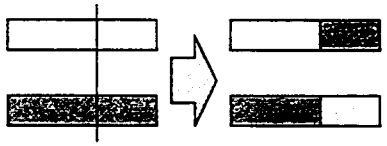
Reconfigurable Hardware

GA (Genetic Algorithm)

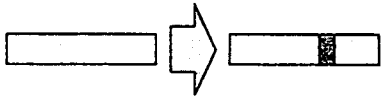
Bio-inspired robust search and adaptation



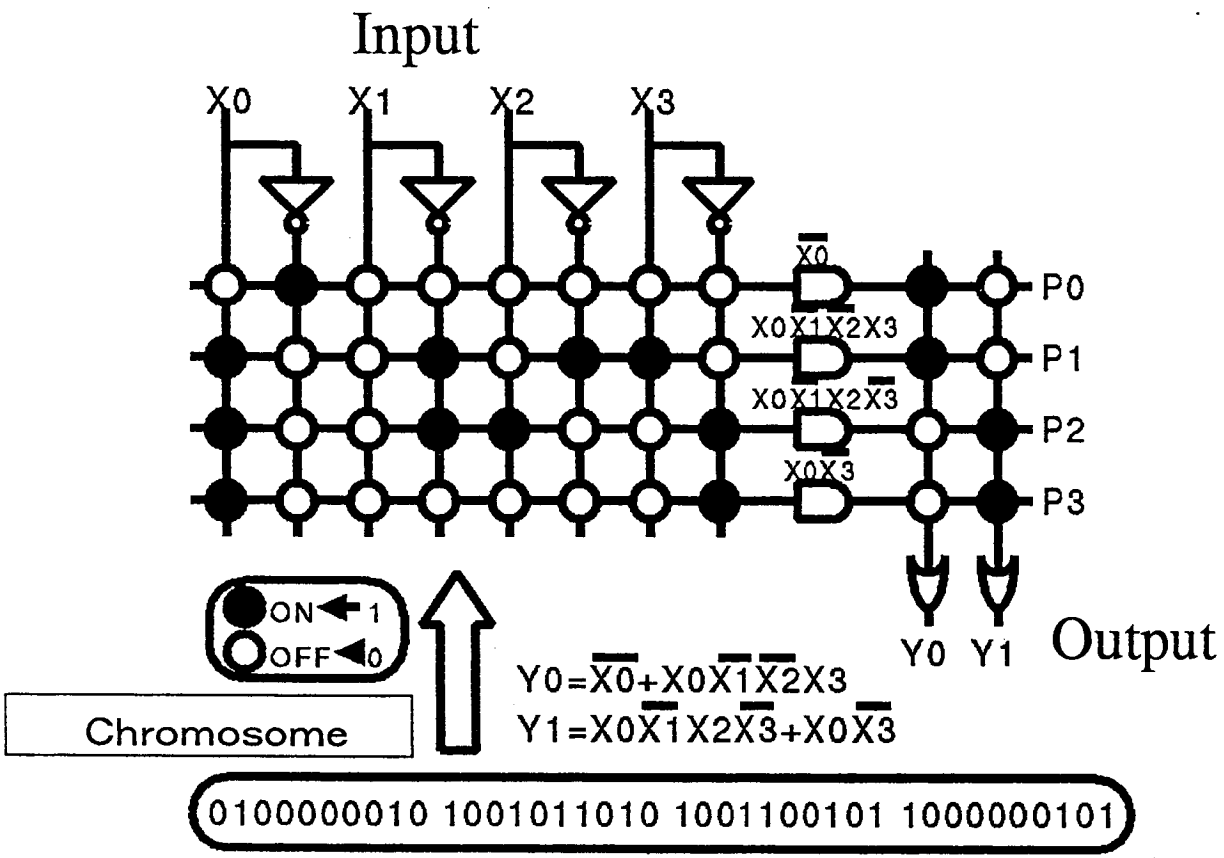
- Selection
  - select high-fitness chromosomes
- Crossover
  - exchange of chromsomes



- Mutation
  - change of chromsomes

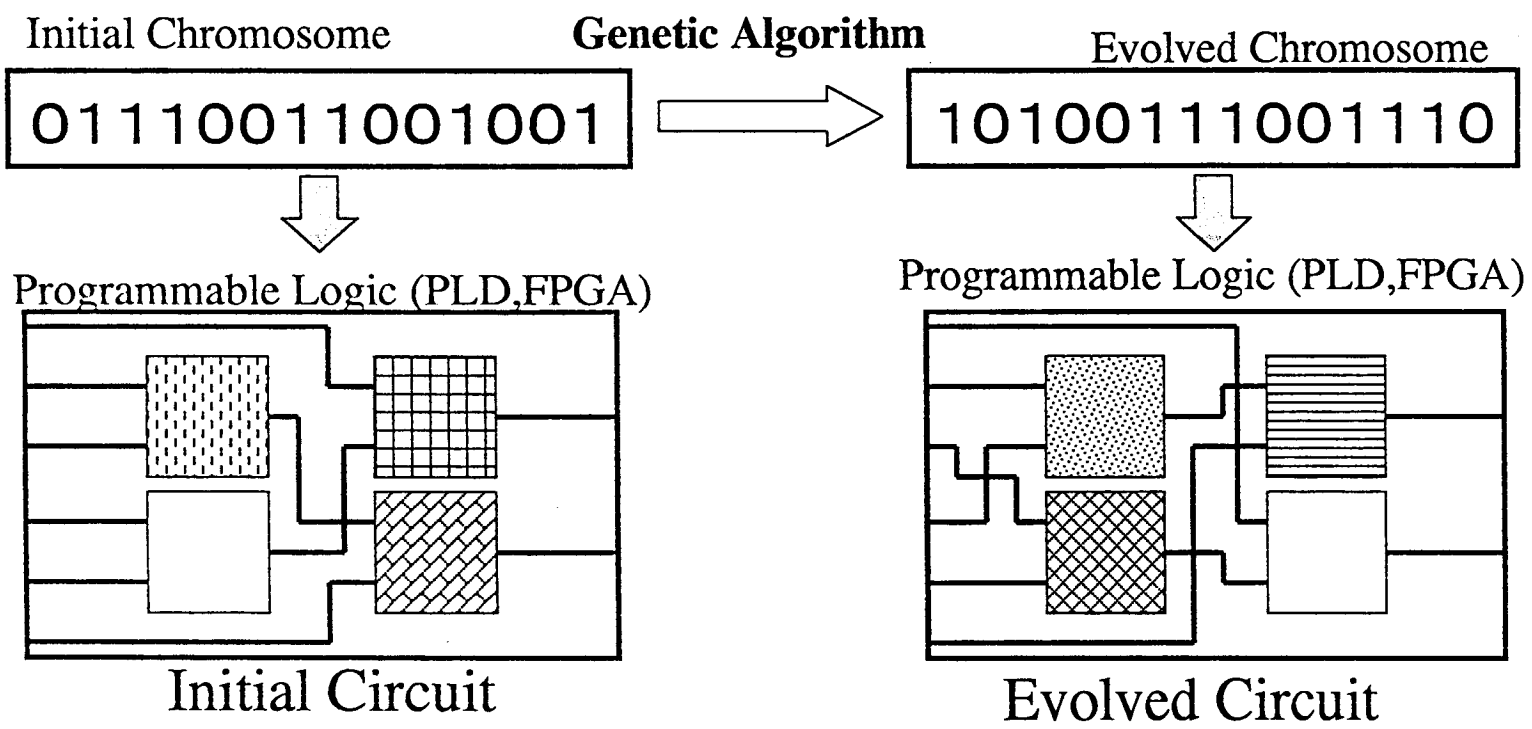


PLA(Programmable Logic Array)



Basic idea of Evolvable Hardware

- EHW= Genetic Algorithms + Programmable Logic



Digital Hardware Evolution

- Chromosome determines:
  - types of hardware components
  - interconnections among hardware components
- Gate-level hardware evolution
  - Hardware components are primitive gates such as AND-gate and OR-gate.
- Function-level hardware evolution
  - Hardware components are higher hardware functions such as adders and multipliers.

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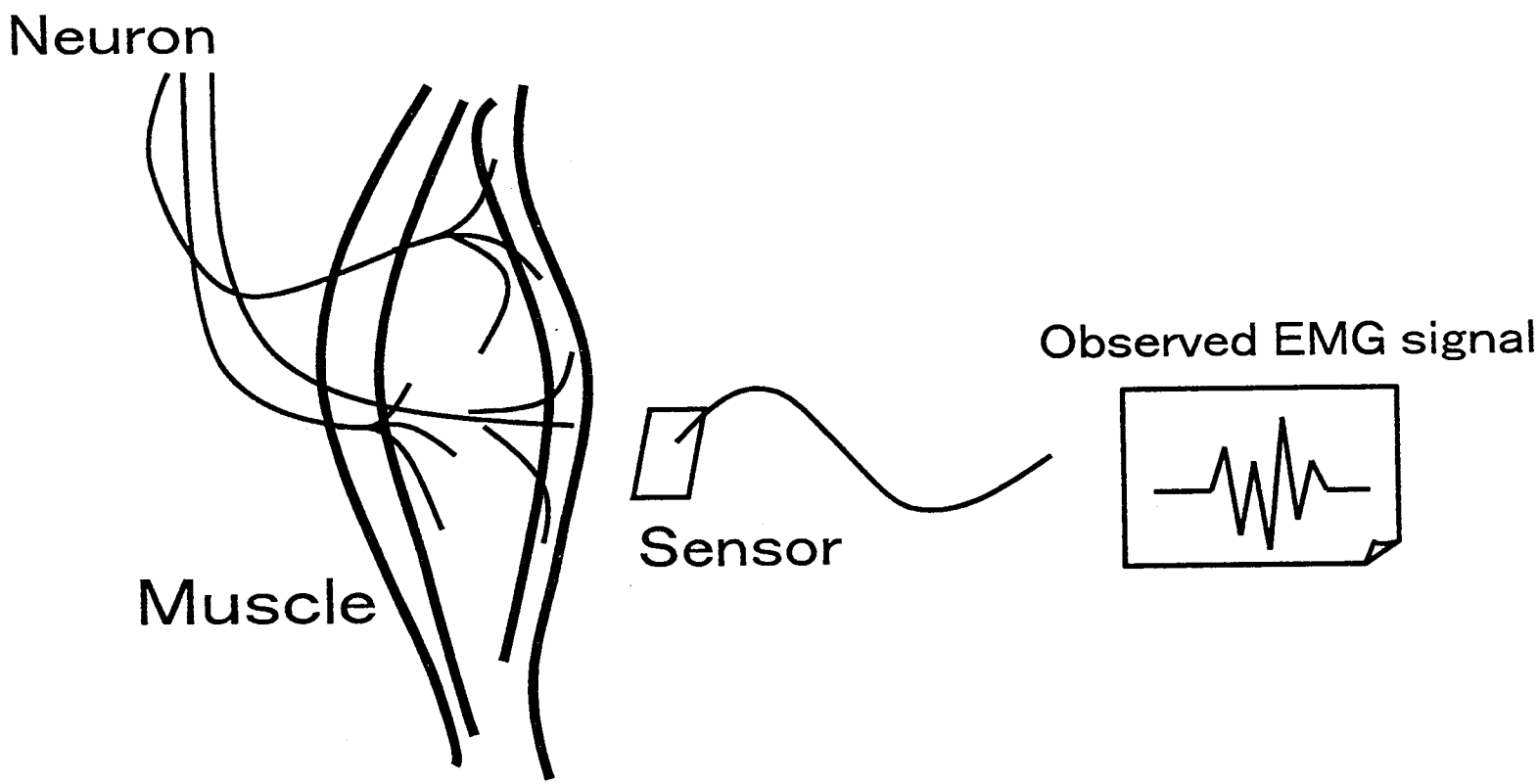
EMG Prosthetic Hand

- EMG(electromyograph)
  - operated by remaining muscles
- Control of hand feels natural
  - same feeling as the hand was available

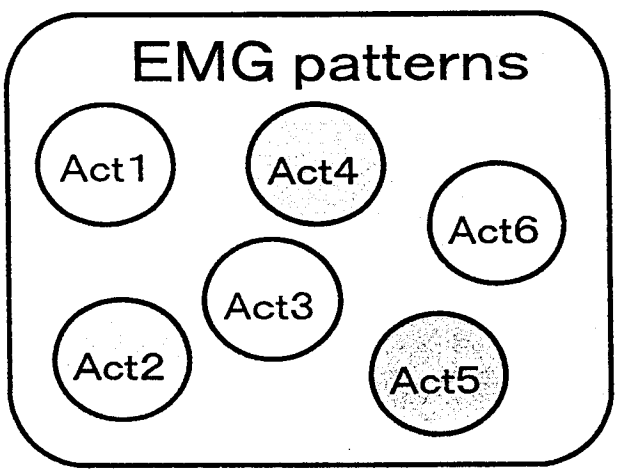
⟺ body－powered hand

EMG(Electromyography)

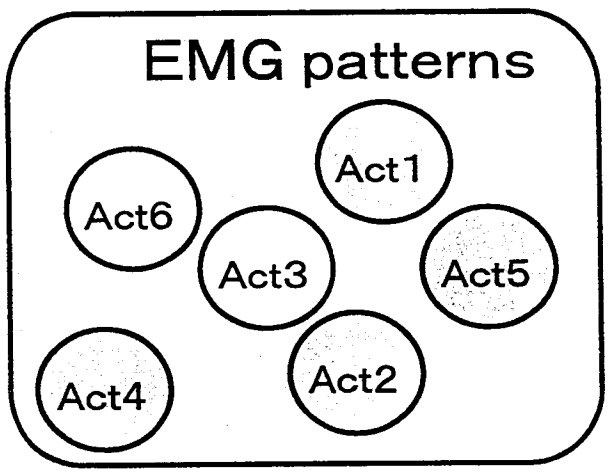


EMG characterestics

- Specific to individuals
- Depends on muscle conditions
- Depends on sensor positions



Mr. A



Mr. B

Needs of adaptation

- EHW implements a pattern recognition hardware specific to individuals.
- Boolean logic can implement a noise－insensitive pattern recognizer.

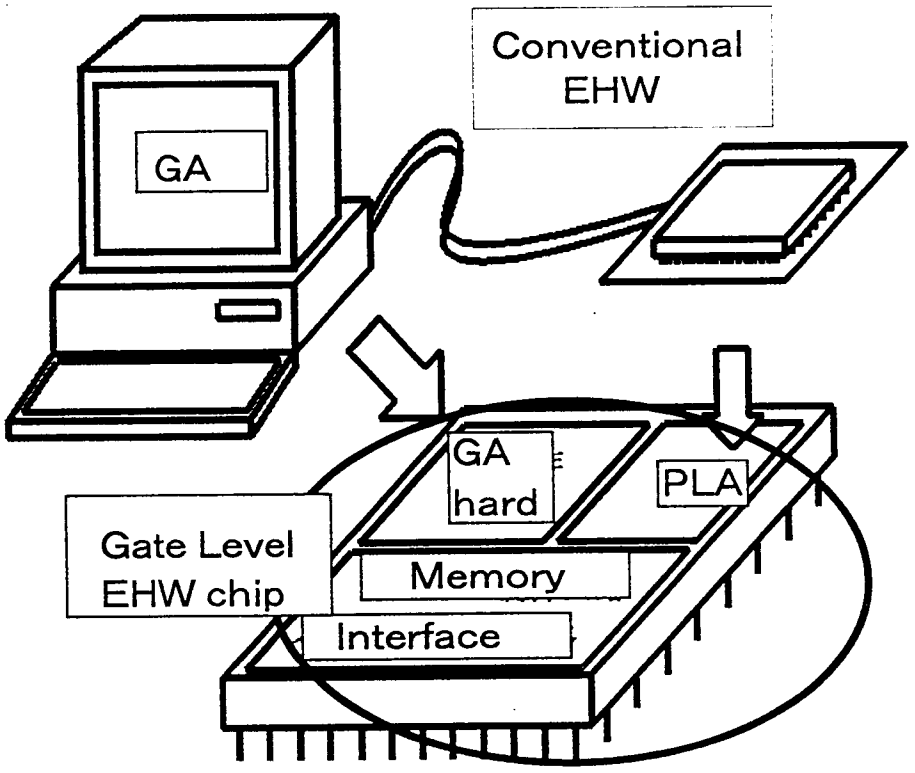
⇩

- EMG hand can adapt to individuals very quickly by EHW chip (5min).

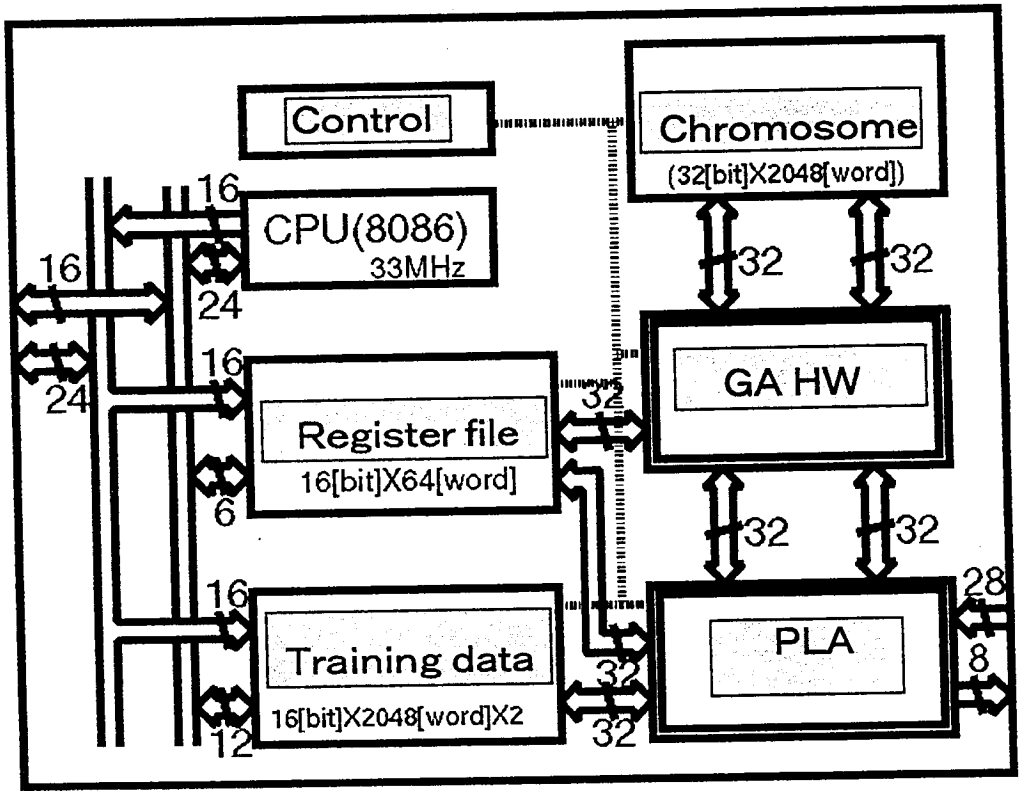
Gate Level EHW Chip

- Integration of GAhardware and PLA into a chip

- Compact
- Fast



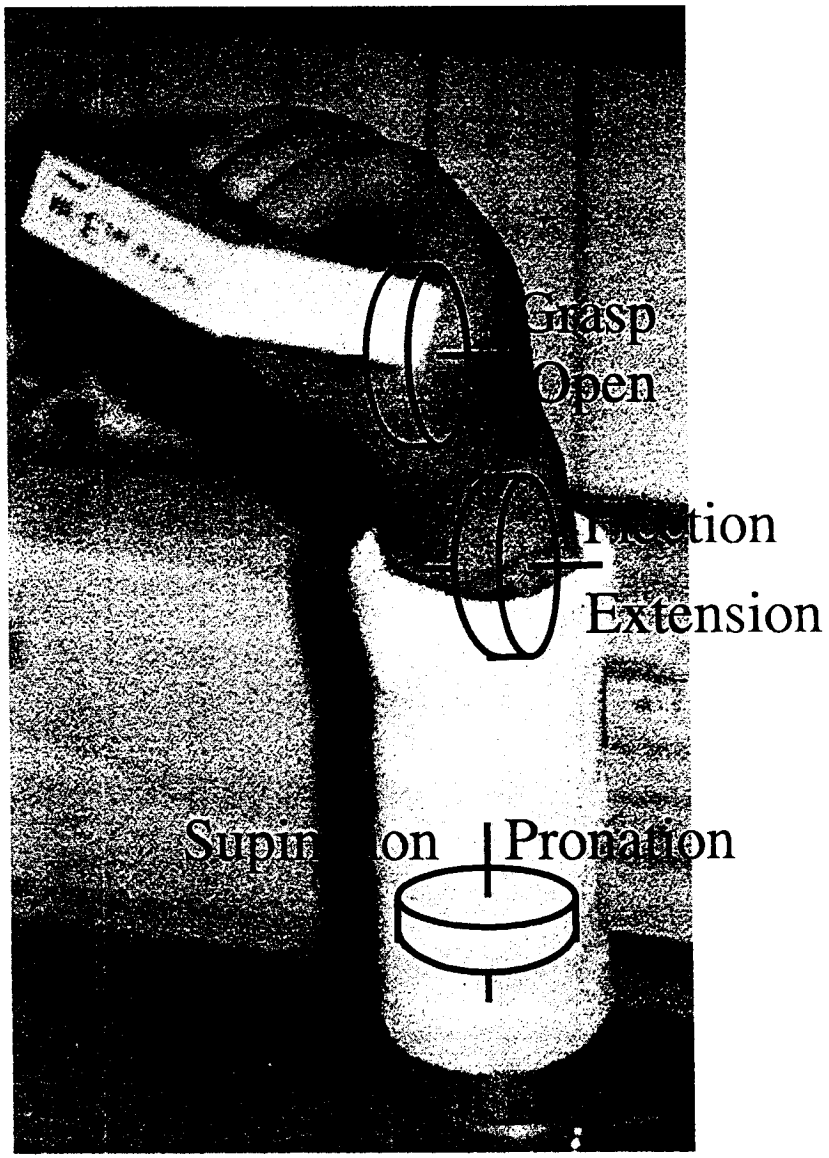
EHW chip v1 block diagram



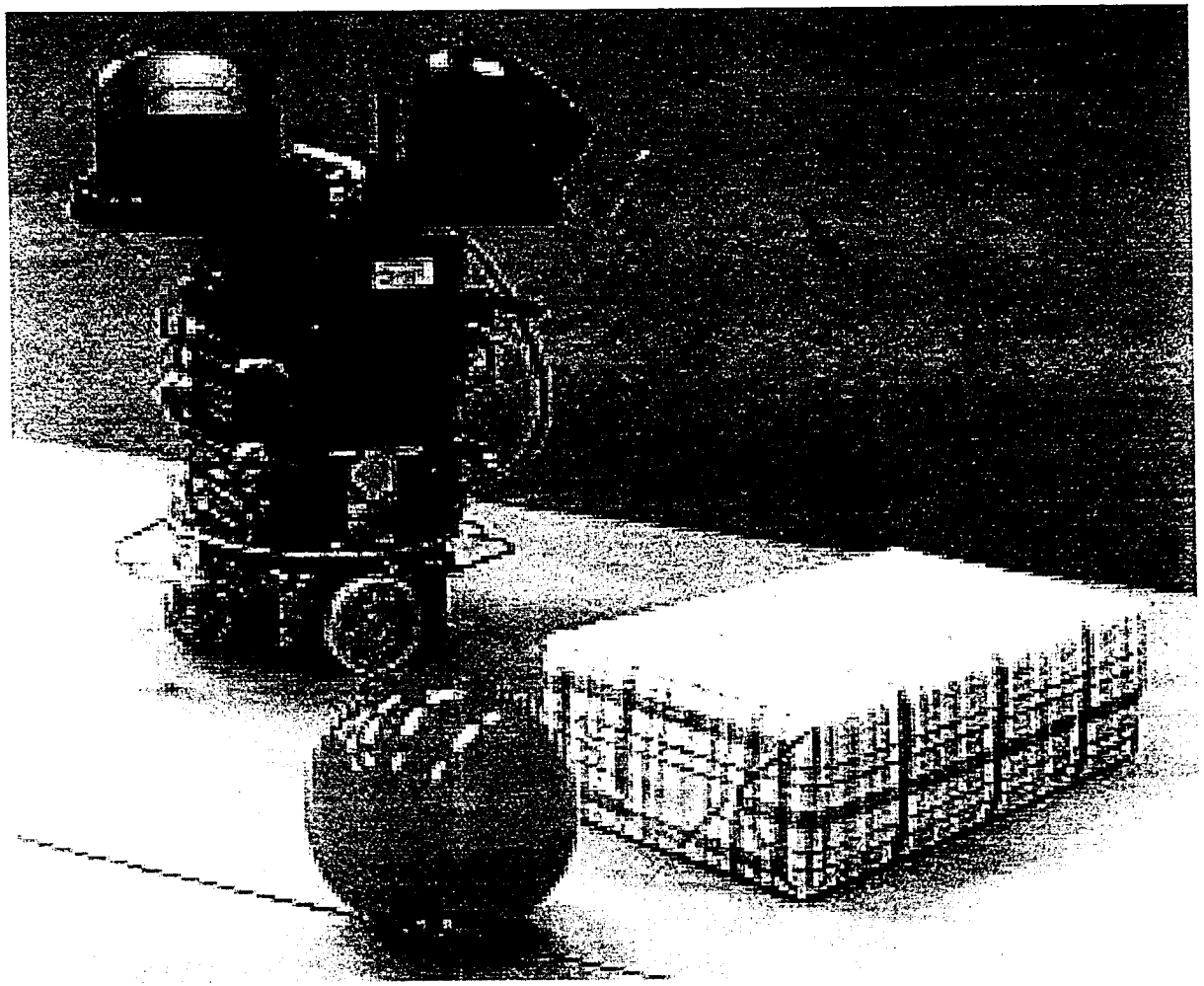
EMG hand

3 degrees of freedom,

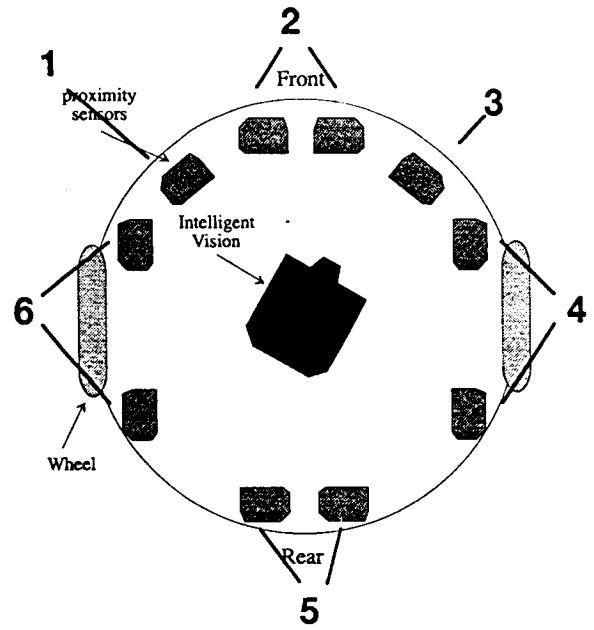
6 movements



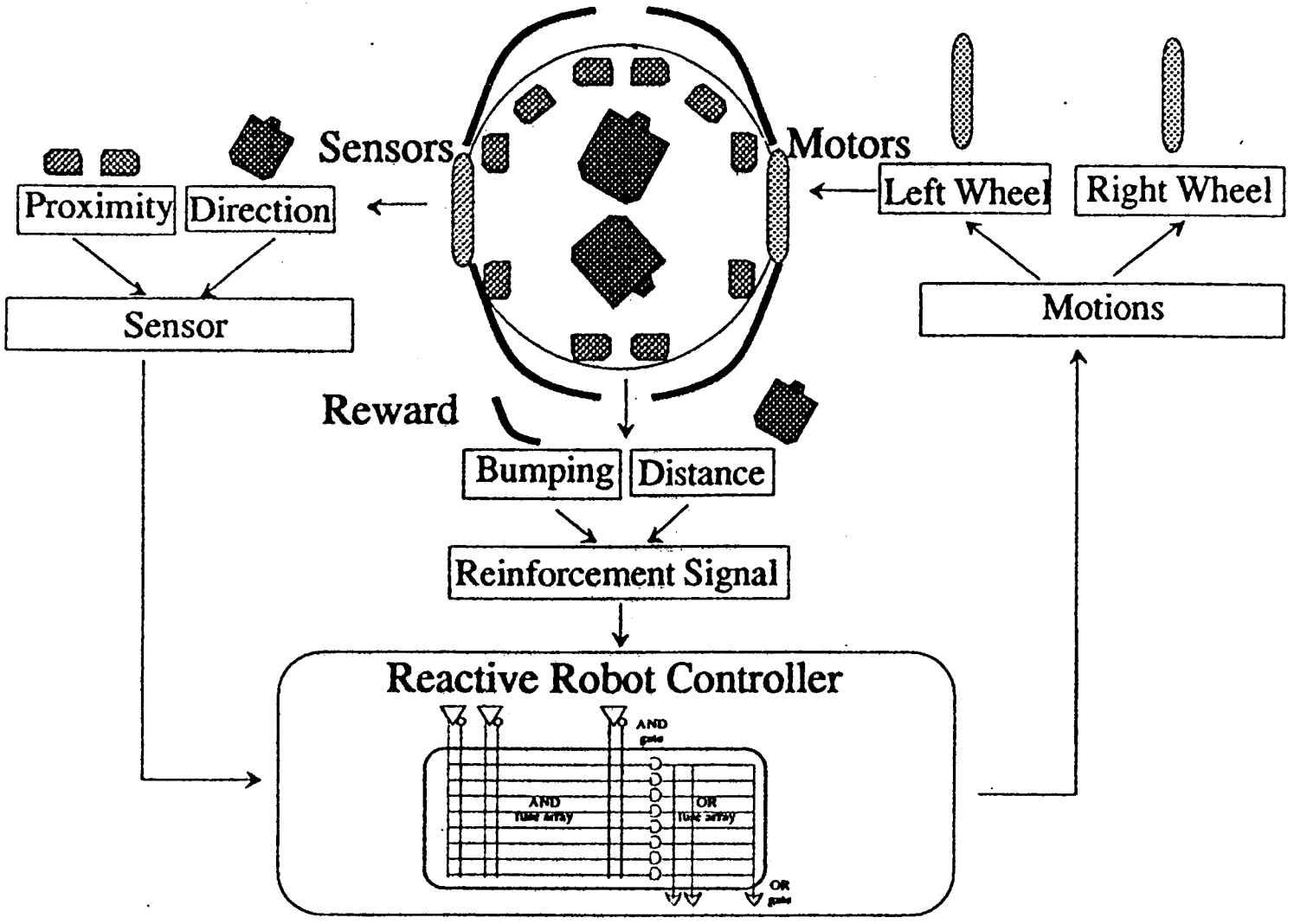
A autonomous mobile robot EVOLVER



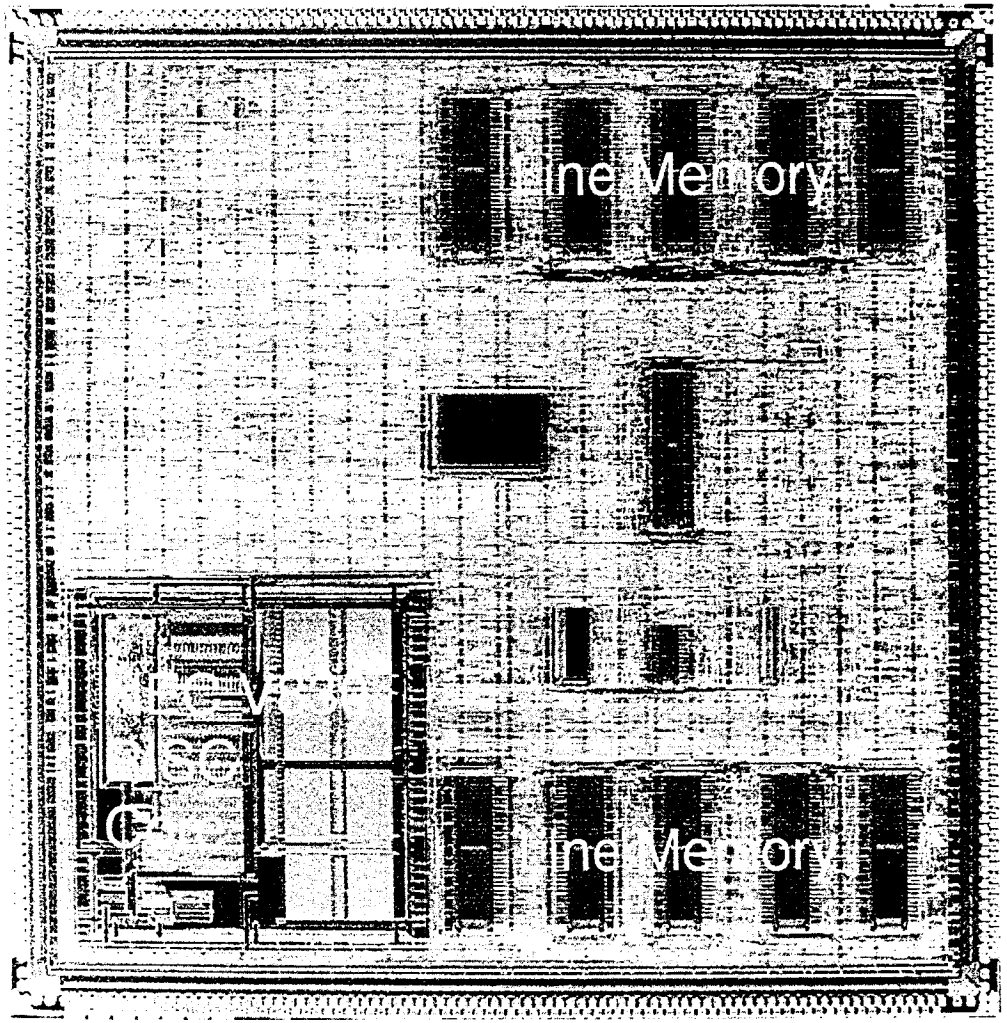
ETL Robot



- **Sensors**
  - **6 Infra-red sensors:** On-Off with 30 cm sensitivity for obstacle avoidance
  - **2 Tracking Cameras:** for tracking colored target
- **Motors:**
  - **2 motor- wheels at both sides driven independently**
  - **Controlled by speed**

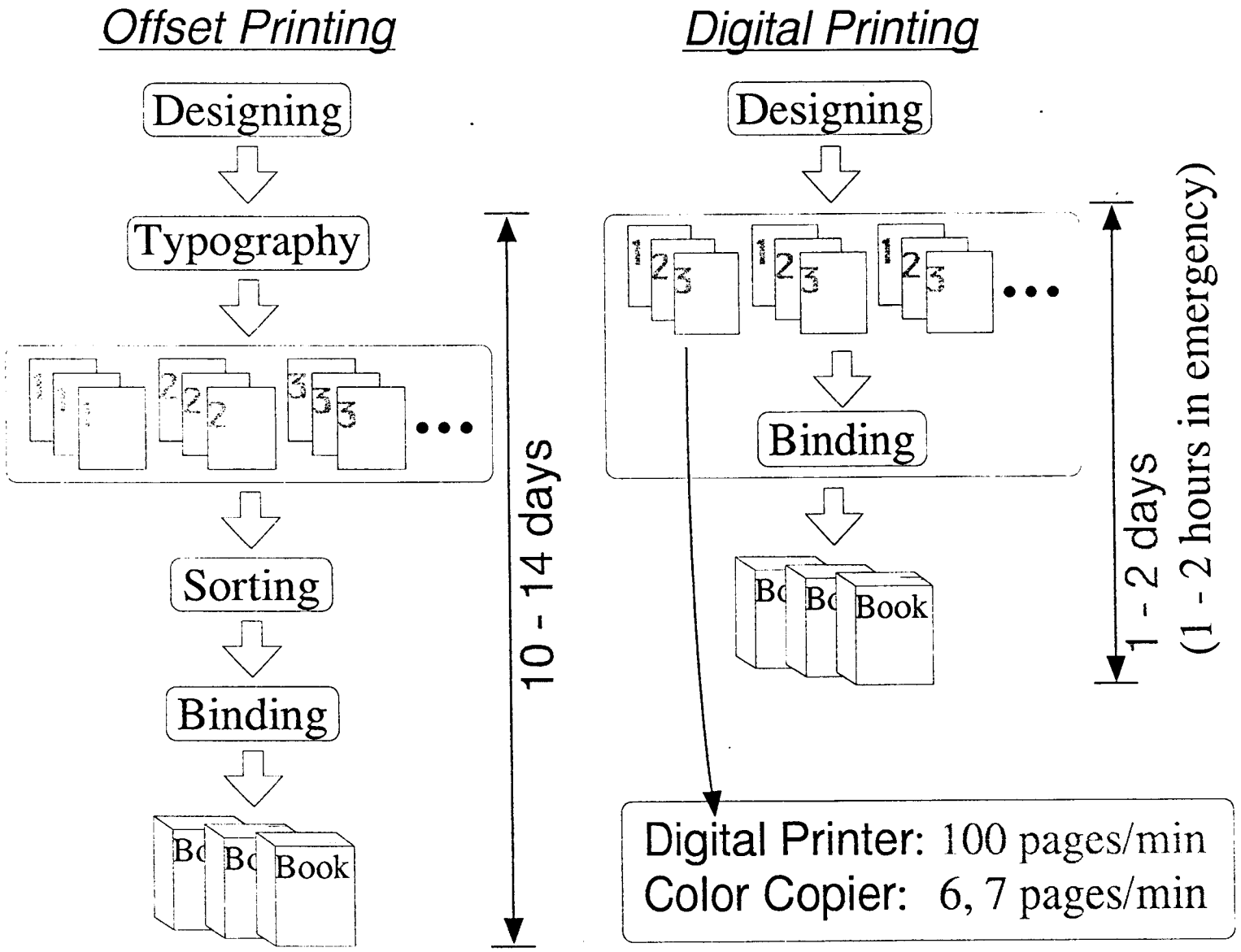

Sensors
Motors
Proximity
Direction
Left Wheel
Right Wheel
Sensor
Motions
Reward
Bumping
Distance
Reinforcement Signal
Reactive Robot Controller
AND gate
AND rule array
OR rule array
OR gate

Data Compression EHW Chip



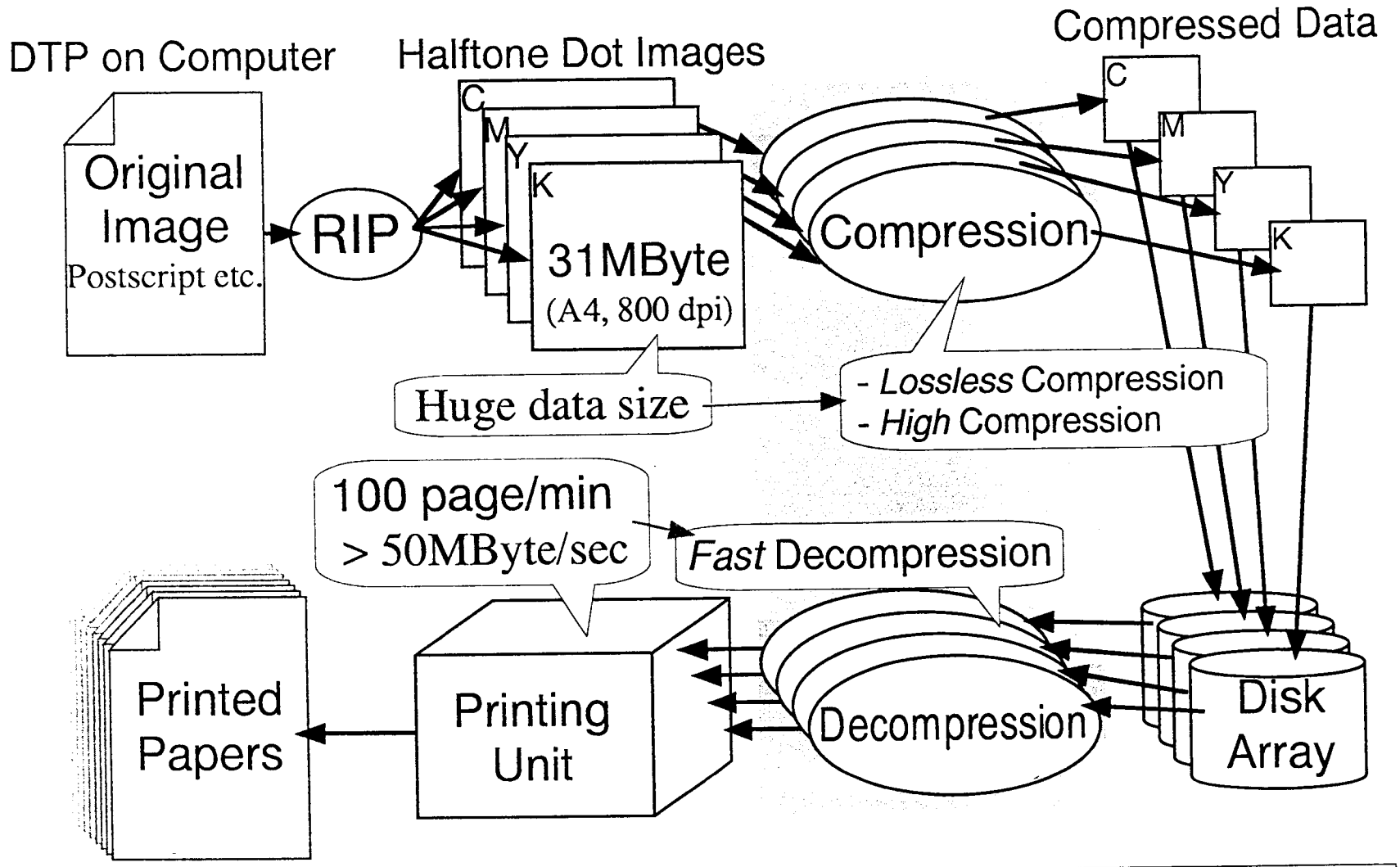
Digital Printing

Latest Generation System in Publishing and Printing Industry



Data Compression for Digital Printing

Heavy costs for Data Transfer & Storage



Data Compression is an effective technique to reduce heavy costs

Results

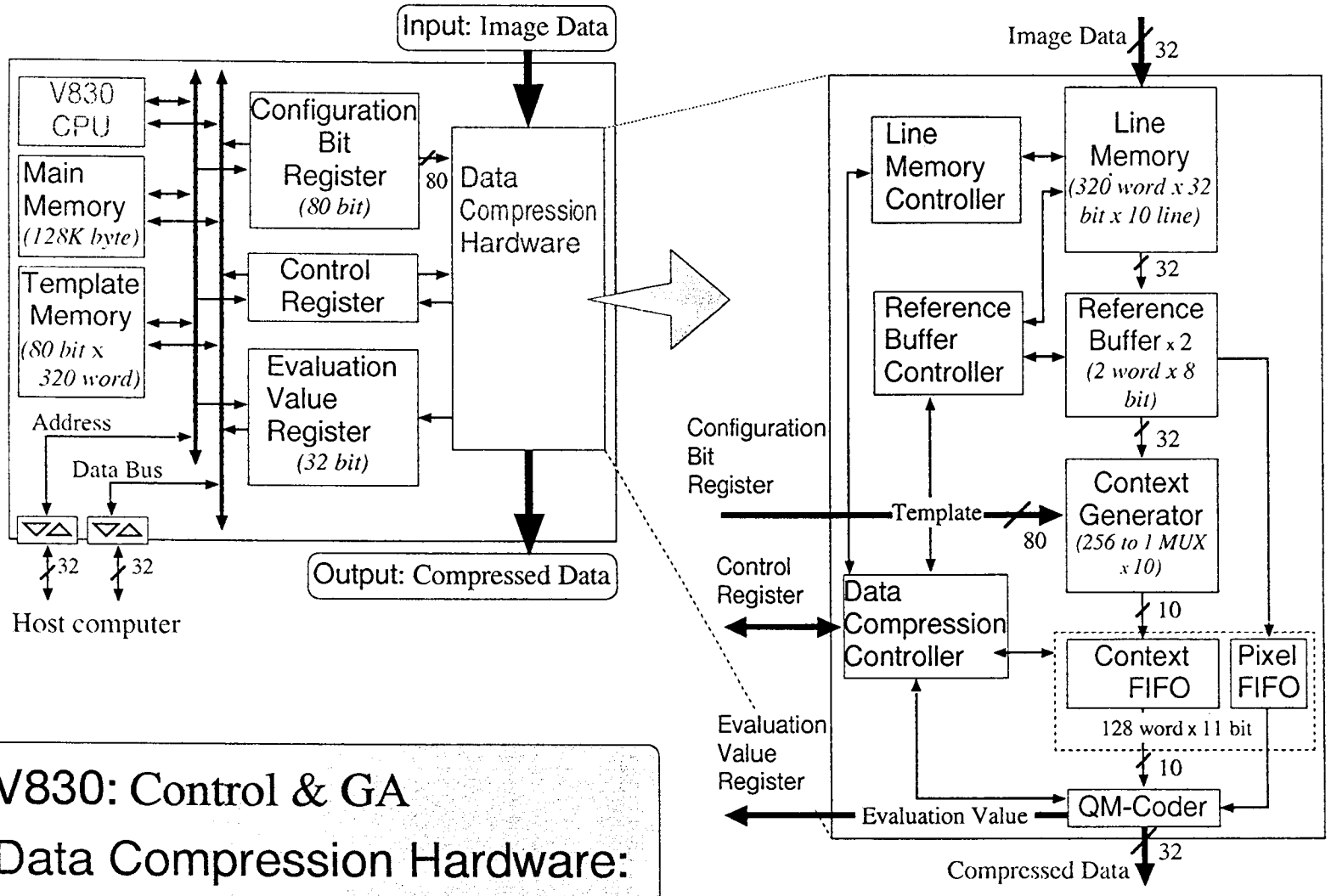
Printer Images: JIS/ISO Standard Color Images

Compression Ratio of EHW is about twice better than JBIG

Compression Ratio

		gzip	JBIG	EHW	
				Simple GA	**Enhanced Representation**
1	C	5.20	6.65	10.18	**10.66**
	M	5.18	7.29	10.11	**10.21**
2	C	3.27	4.61	6.31	**6.36**
	M	3.23	4.78	5.92	**6.06**
3	C	5.54	6.76	13.89	**14.08**
	M	4.84	6.33	10.55	**10.66**
4	C	5.49	7.79	11.40	**11.84**
	M	5.12	7.67	10.47	**10.77**
5	C	5.28	7.18	11.34	**11.59**
	M	4.85	6.60	9.91	**10.25**
6	C	9.72	10.08	25.61	**26.07**
	M	7.98	10.04	18.75	**19.36**
7	C	4.67	5.81	9.32	**9.36**
	M	4.22	6.05	8.01	**8.08**
8	C	3.13	4.46	5.84	**5.89**
	M	3.26	4.63	5.77	**6.00**
Average		5.06	6.67	10.83	**11.08**

Architecture of Data Compression EHW Chip



V830: Control & GA

Data Compression Hardware:

Compressed Data

Evaluation function of GA

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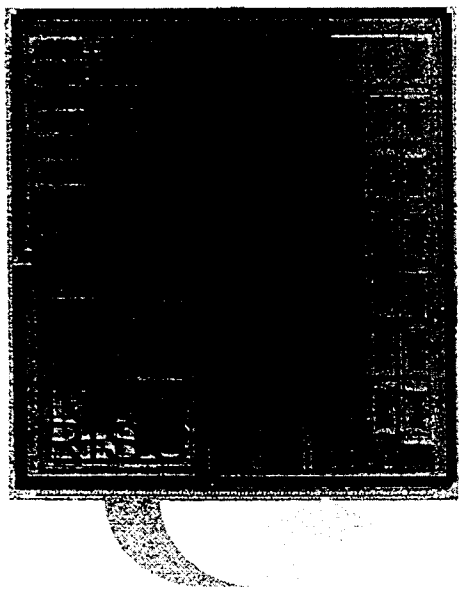
Genetic Reconfiguration of DSPs Chip (GRD chip)

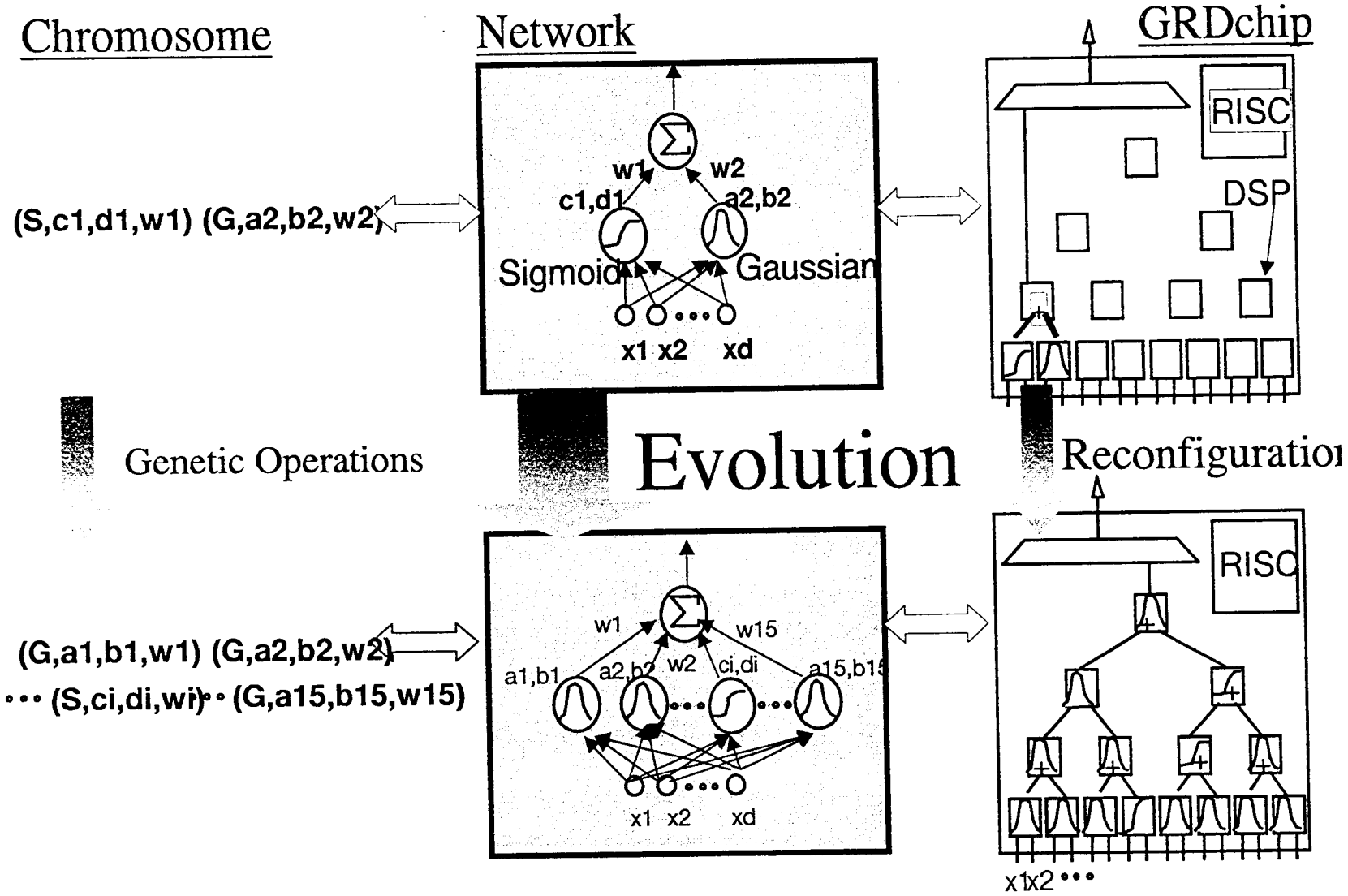


reconfiguration

(13.5mm x 13.5mm)

- Autonomously reconfigurable Neural Network chip
- 100Mhz 32bit RISC core + 33Mhz 16bit DSP x 15
  - RISC : GA, reconfiguration, I/O
  - DSP : execution of NN, Steepest Descent Method
  - scalable connection of the chips

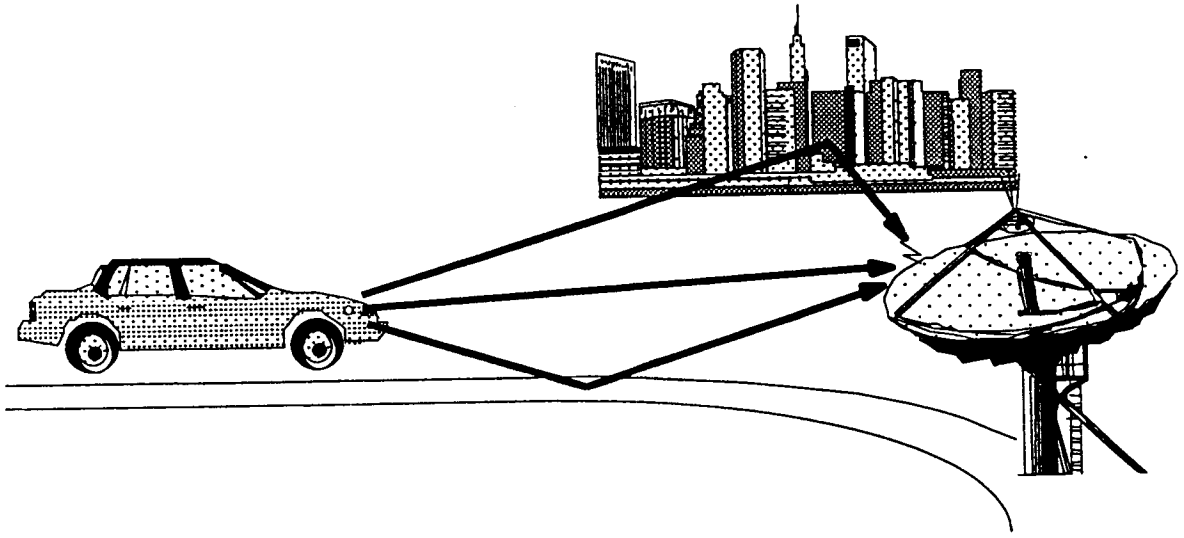
GRD chip: basic concept



Performance of GRD chip

- Operational since last June
- second version in progress
- 10 times faster than Pentium II (400MHz)
- 200 times faster thanSUN Ultra2
  (with 9 GRD chips)
  - Execution speed per chip
    319MCPS (Mega Connection Per Second)

Adaptive Equalization



- Adaptive Equalization
  - On-line learning is needed to adapt to the changing environment.
- Fast speed and compact implementation by hardware.

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Analogue EHW chip for cellular phones

- Off-line analogue EHW
- Intermediate Frequency Filter
  - Analogue Band-pass Filter
  - Must be compact and fast: LSI required
  - Large market
- Variations in analogue components performance are adjusted by GA.

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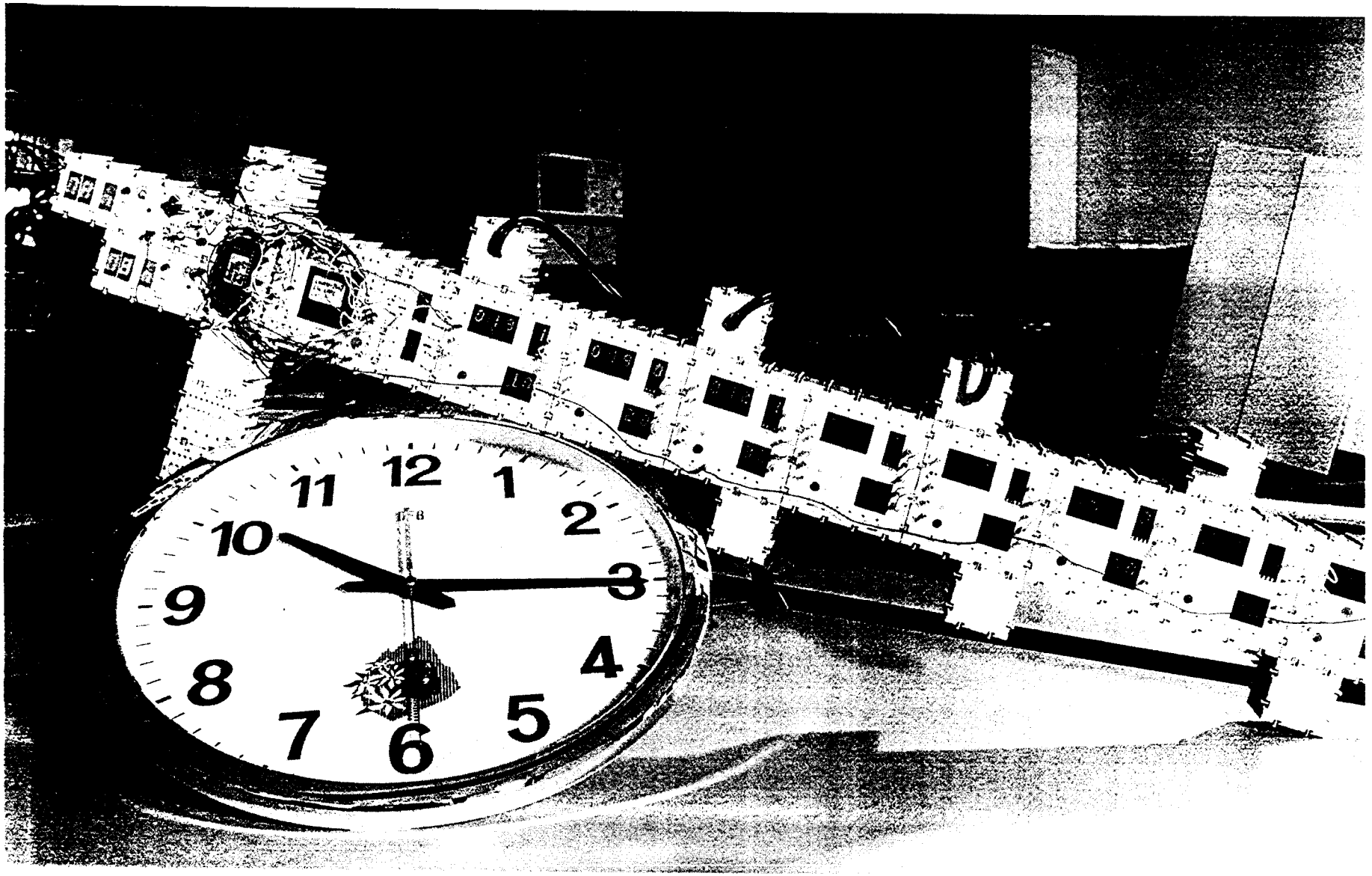
Research Trend (1)

- Bio-inspired machines
  - Swiss Federal Institute of Technology
    - The Firefly machine
    - Ontogenetic Hardware: The Bio Watch
  - ATR
    - CAM Brain


12
1
2
3
4
5
6
7
8
9
10
11

Research Trend (2)

- Digital Evolvable Hardware
  - University of Sussex
    - Evolvable Robot Controller
    - Frequency discriminator on FPGA
  - NTT Communication Science Laboratory
    - Hardware Evolution System AdAM based on HDL
  - CSEM
    - Field Programmable Processor Array
  - Electrotechnical Laboratory

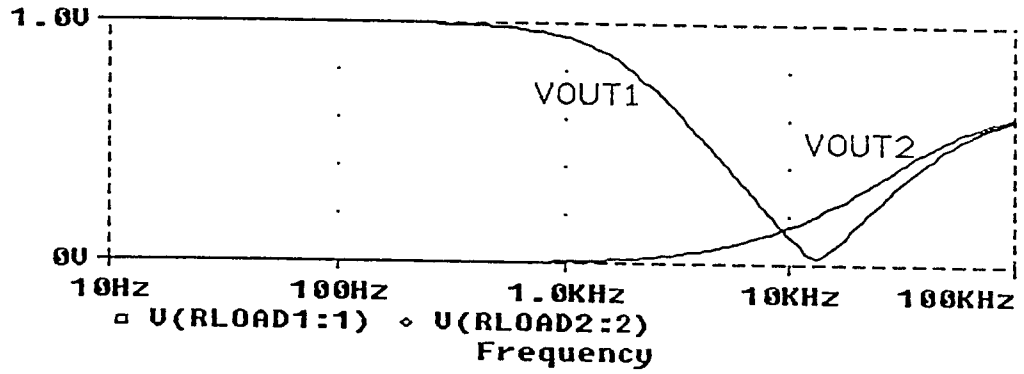


Figure 2 Frequency domain behavior of best circuit of generation 0.

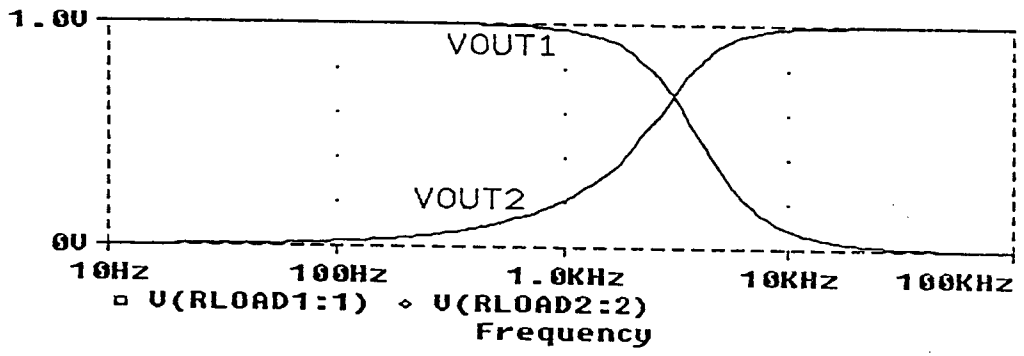


Figure 3 Frequency domain behavior of best circuit of generation 8.

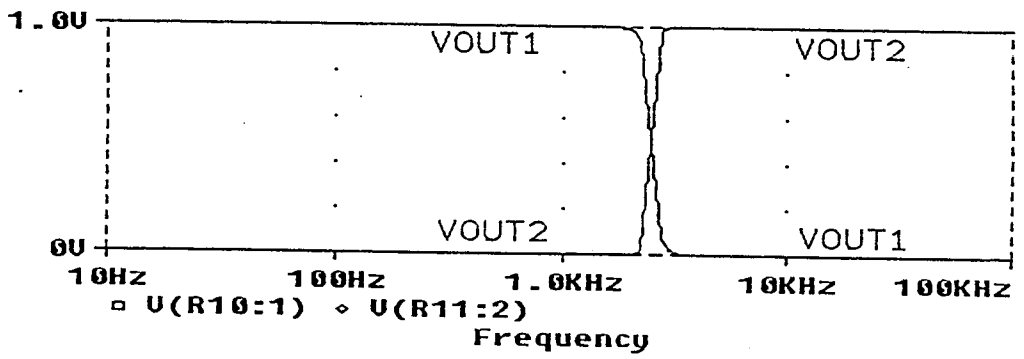


Figure 4 Frequency domain behavior of best circuit of generation

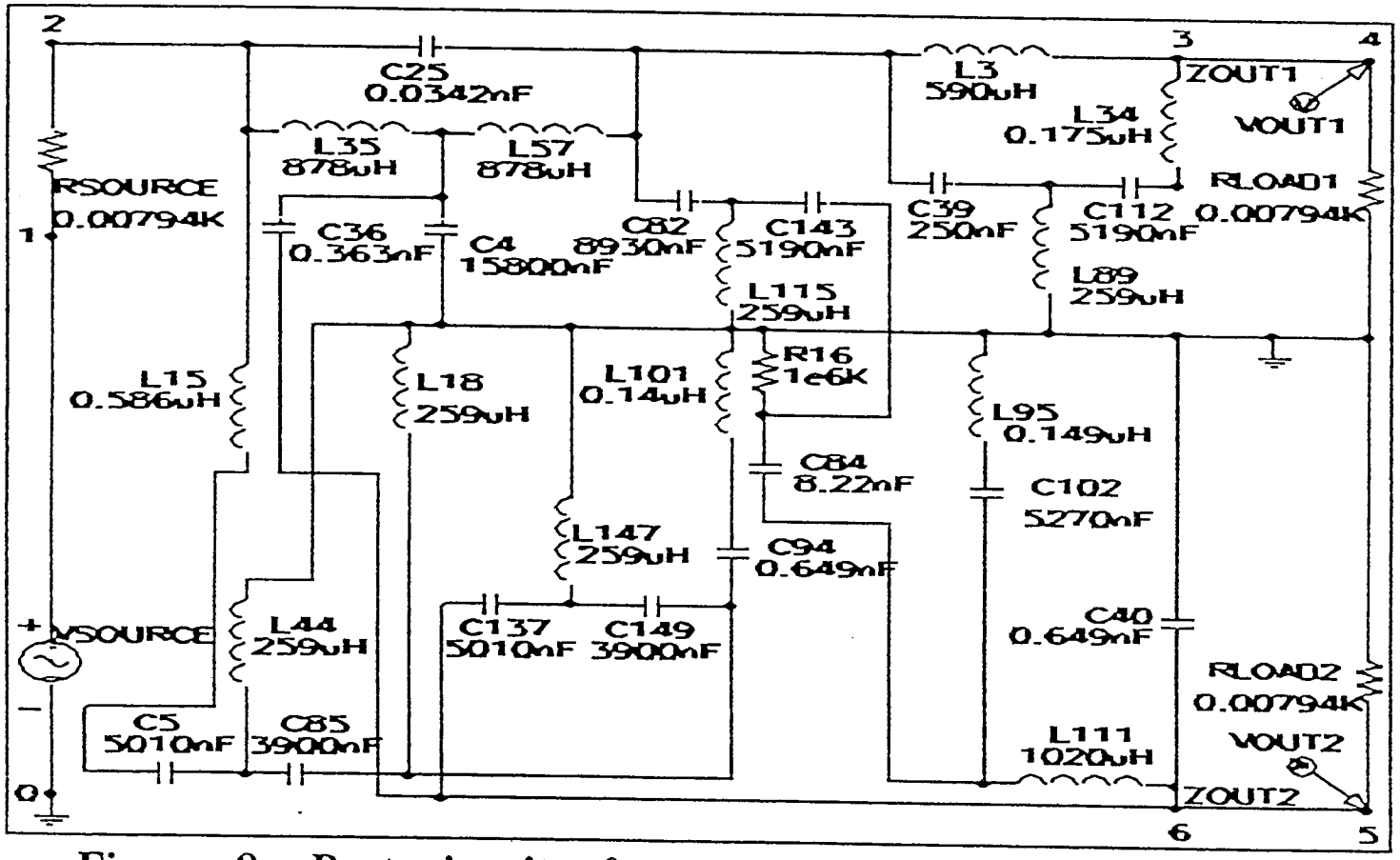


Figure 8 Best circuit of generation 158 after substitution.

Conclusion

- Industrial Applications for EHW
  - Time-variant behaviour (Adaptive)
  - Real-time performance
  - Fault-tolerant
  - Analogue systems
- Promising application domains
  - prosthetic hand
  - data compression
  - analogue devices