

Radiation Hardened PowerPC 603e™ Based Single Board Computer

Presented to

JPL

2 August 2001

Gary R. Brown

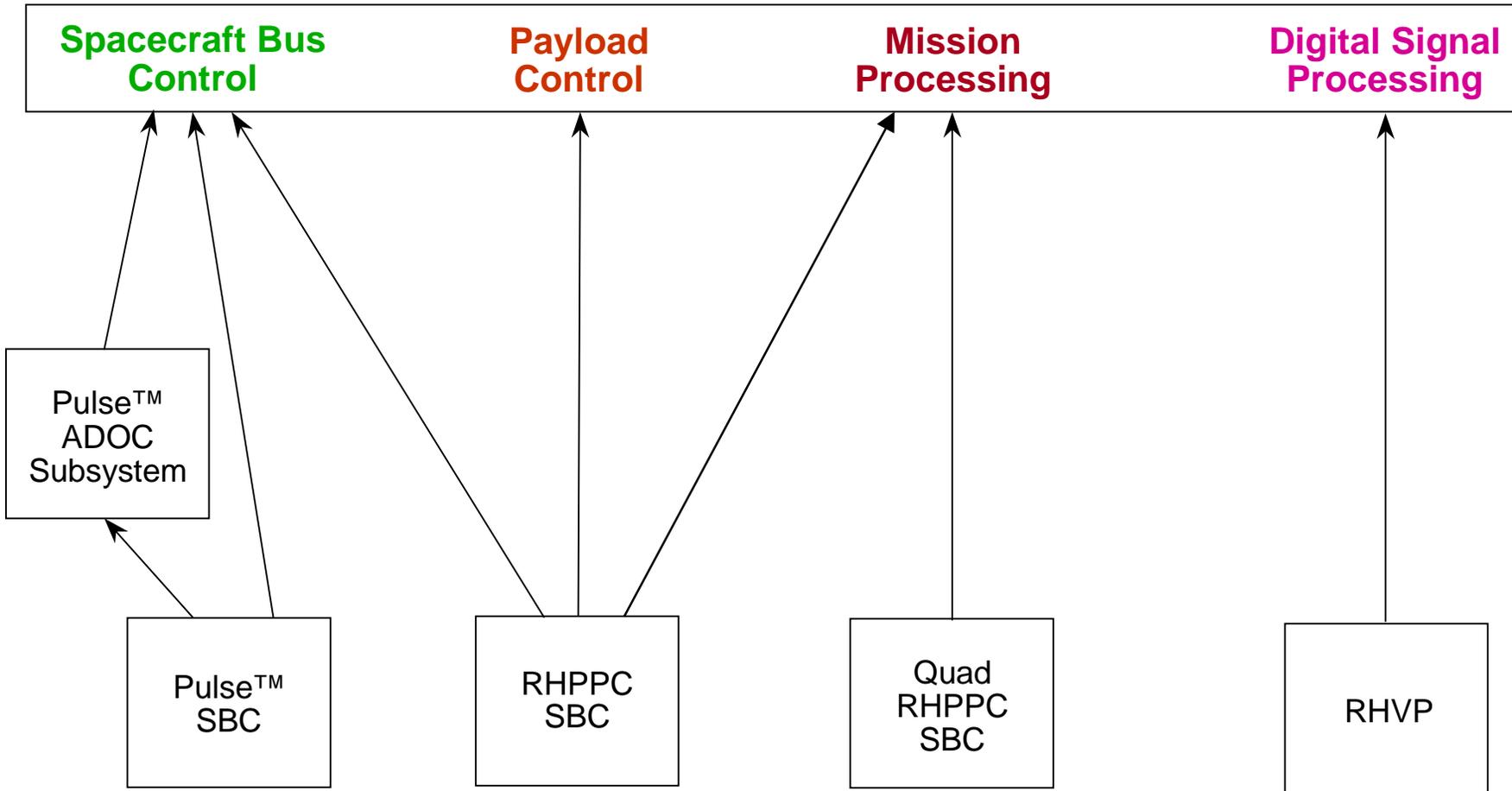
**Honeywell Inc.
Space Systems
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Complete Product Line Offering

Increasing Performance
and MIPS/W



- RHPPC 70 MIPS @ 50 MHz
- 6Ux220, 3.5 lbs, 10W (nom)
- IEEE1394 backplane
- CCSDS telecommand port

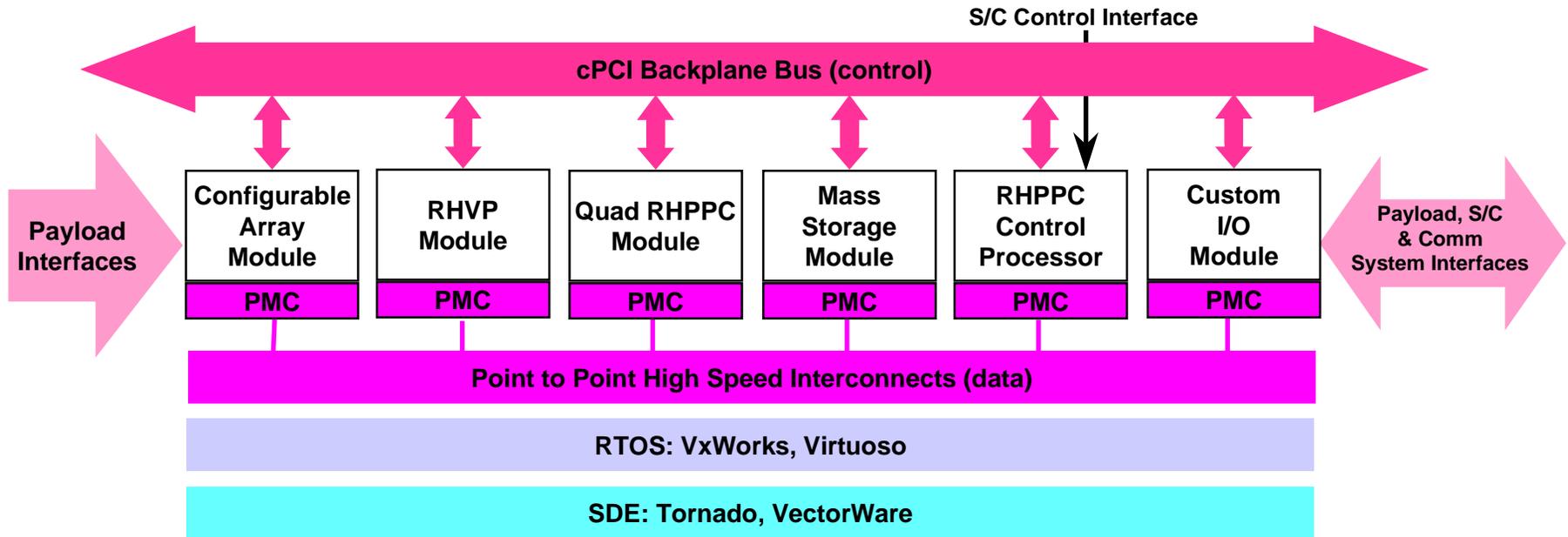
- RHPPC 222 MIPS @ 133 MHz
- 6Ux220, 2.6 lbs, 12.5W (nom)
- cPCI backplane
- 1553 & serial ports

- 4 RHPPC 700 MIPS
- 6Ux220, 2.6 lbs, 20W (nom)
- cPCI backplane
- IEEE1355

- RT21020/RHDSP24
- 2-3 GFLOPS sustained
- 6Ux160, 2.2 lbs, 16W (nom)
- cPCI backplane

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Open Architecture For Payloads

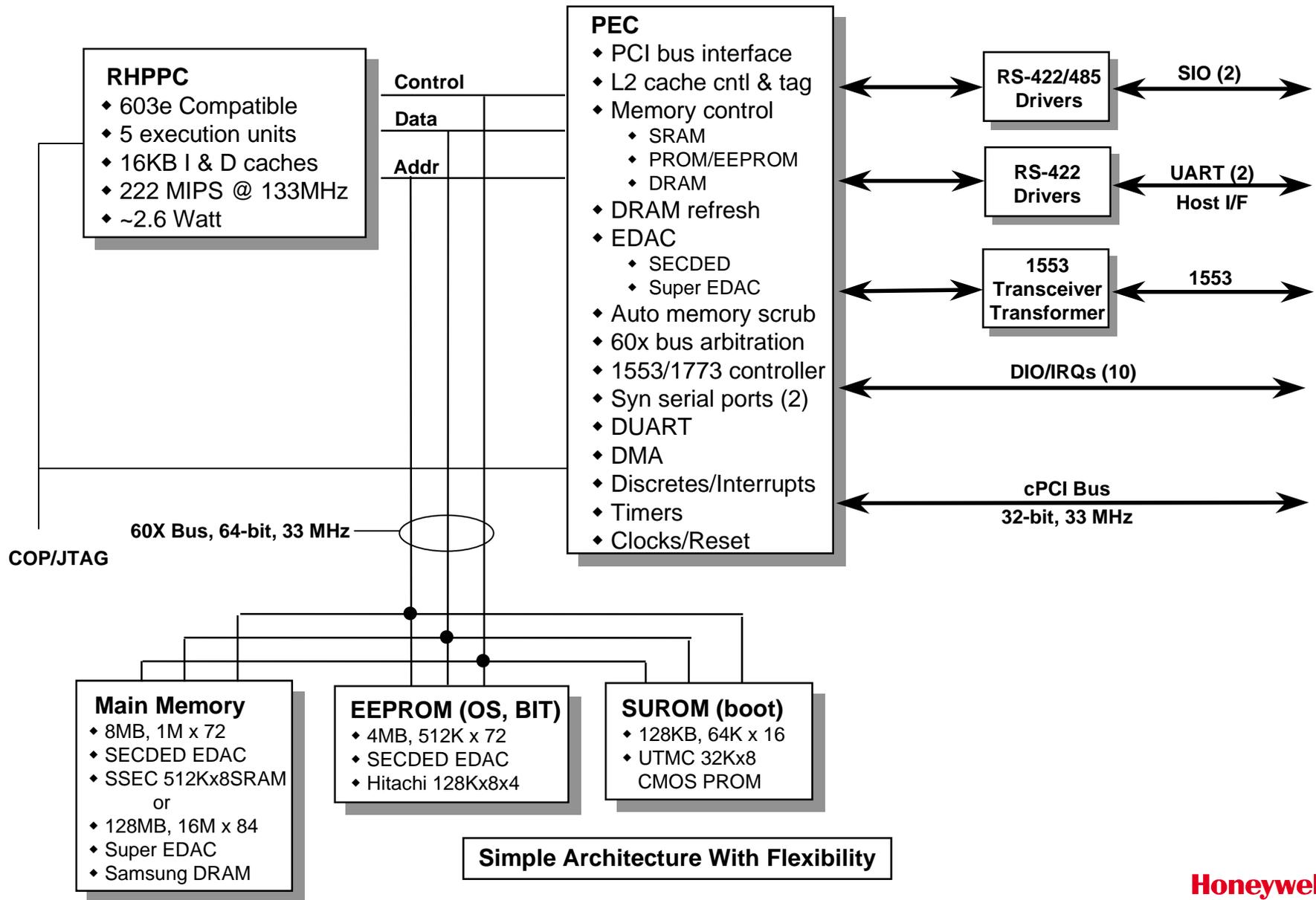


- Highly flexible, scalable, open architecture based on COTS standards:
 - Engines: PowerPC603e™ general purpose, ADSP-21020 DSP, and DSP-24/MMU-24 Vector Processor
 - Software Tools: Wind River Tornado™ 2.0 , VectorWare, pRISM
 - Operating Systems: Wind River Systems VxWorks™ 5.4, Eonic Systems Virtuoso™, pSOS
 - I/O: IEEE-1355 Link Port Serial Interfaces & MIL STD-1553/1773 Command & Control
 - Backplane: cPCI (rev 2.2)
 - Form Factor: Compact PCI (6Ux220) & PMC-like daughter cards
- These building blocks can be mixed/matched to create payload processing solutions.
 - Allows efficient subdivision of a task using data flow model.
 - Open scalable architecture easily accepts any mix of modules and new module types.
- Commercial equivalent hardware modules available for software development.

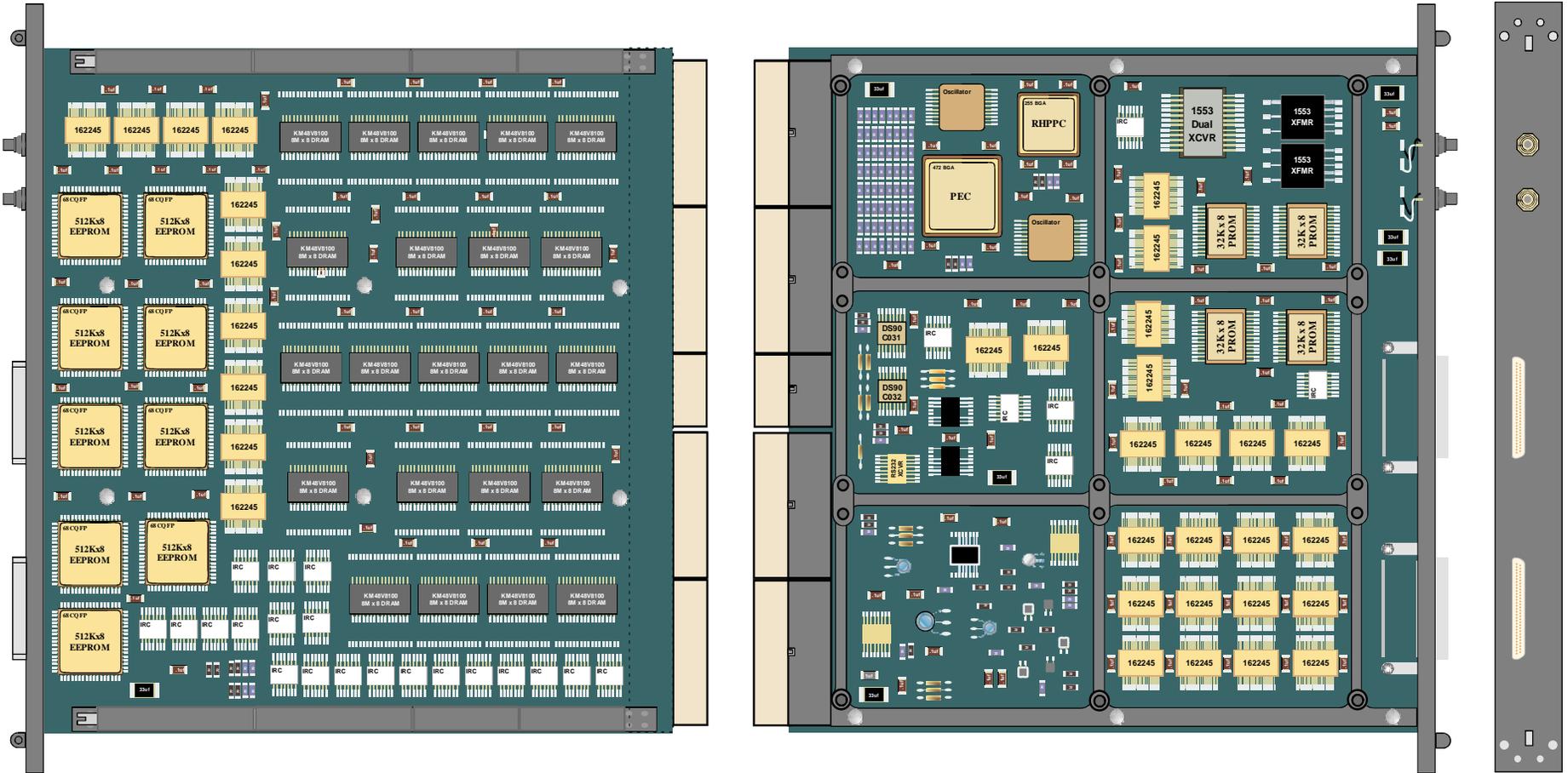
COTS Standards Reduce Cost & Risk

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Payload Controller SBC Block Diagram



Payload Controller SBC Mechanical Design



- 6U x 220 (9.187" x 8.661"), 2.6 pounds (1165 gr), 11W (nom)
- Same cPCI backplane connectors as used by X2000 (JPL)
- Standard face panel with 2 1553 connectors & I/O connectors

cPCI Standard Form Factor

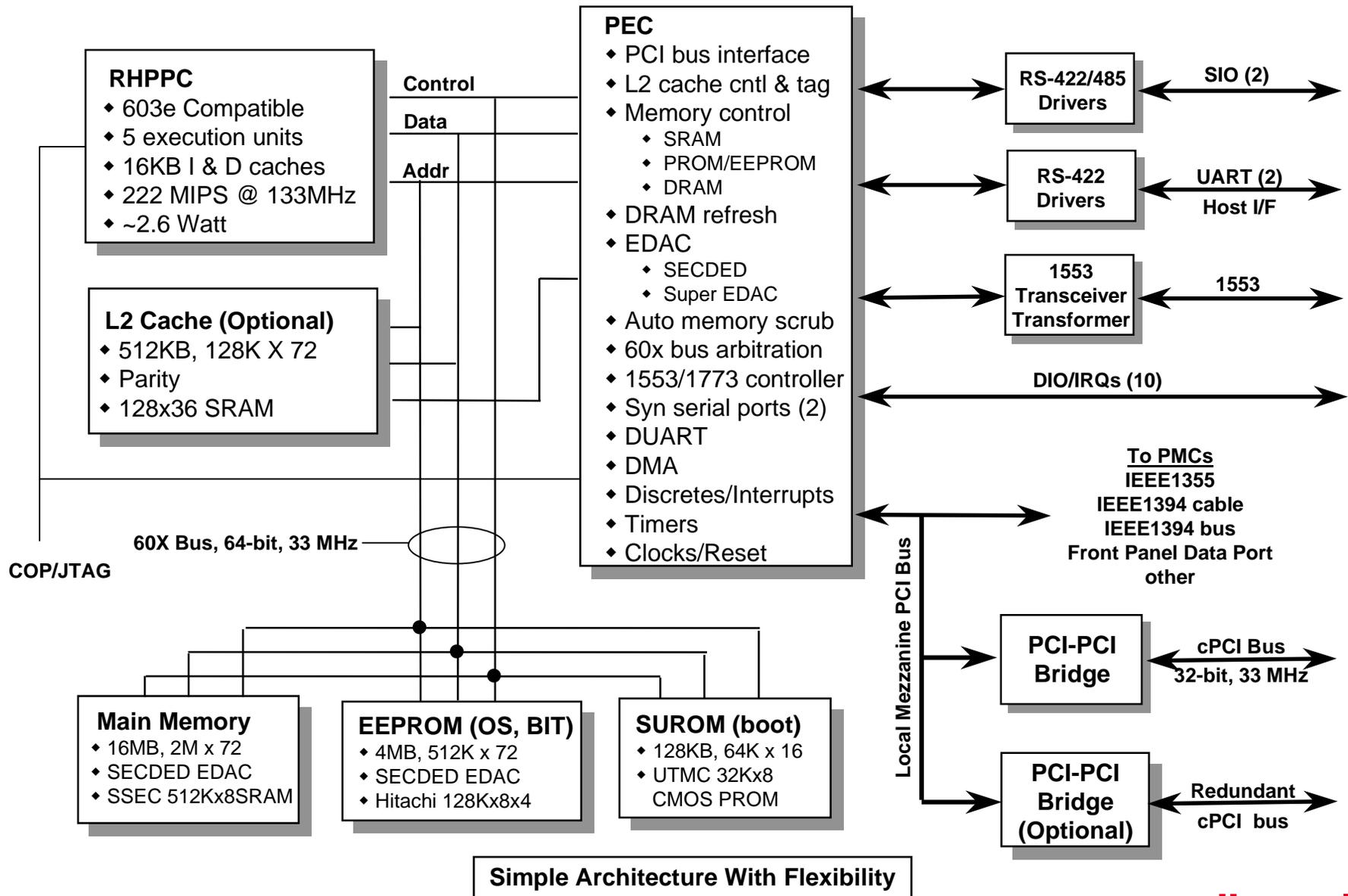
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Payload Controller SBC Features

- 6U x 220mm (9.187" x 8.661"), 2.6 pounds, 11W (nom)
- 222 DMIPS @ 133 MHz RHPPC processor (cache: 32KB L1)
 - PowerPC 603e™ technology licensed from Motorola
 - 33 MHz 60x bus, 64 bit data + EDAC, 32 bit address + parity
 - Power scalable with clock speed
- Memory
 - 8Mbyte SRAM, SECDED EDAC or 128Mbyte DRAM, super EDAC
 - 4Mbyte EEPROM, SECDED EDAC
 - 128Kbyte PROM (SUROM)
- Backplane: cPCI, 33MHz, 32-bit, 3.3V
- I/O
 - 1553B with 8Kx16 buffer memory, transformer coupled (upgradable to dual rate 1773 with PWB mod)
 - 2 full duplex UART ports, 8250 & 16450 protocol compatible, 9.6K to 1M baud (16 bit rate register)
 - 2 full duplex synchronous serial ports, date/clock/sync, 1.25Mbps or 12.5Mbps (@50MHz)
 - DMA controller for serial I/O and another DMA for mem-to-mem or mem-to- PCI
 - 10 lines programmable as discrete in, discrete out, or interrupt in
 - JTAG/COP debug port
- Timers: 5 general purpose, 2 stage watchdog, mission (20 year)
- Commercial and Military space rad hard
 - TID > 1E5 rad (SRAM)
 - SEU rate < 4.8E-5 e/d (Adams 90% WC, GEO)
 - Dose rate upset > 1E8 rad/s
 - No latchup
- -40°C to 80°C rail temp, 20 Grms
- Ps > 0.99, 15 year, 35°C (with cold spare)

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Payload Processor SBC Block Diagram



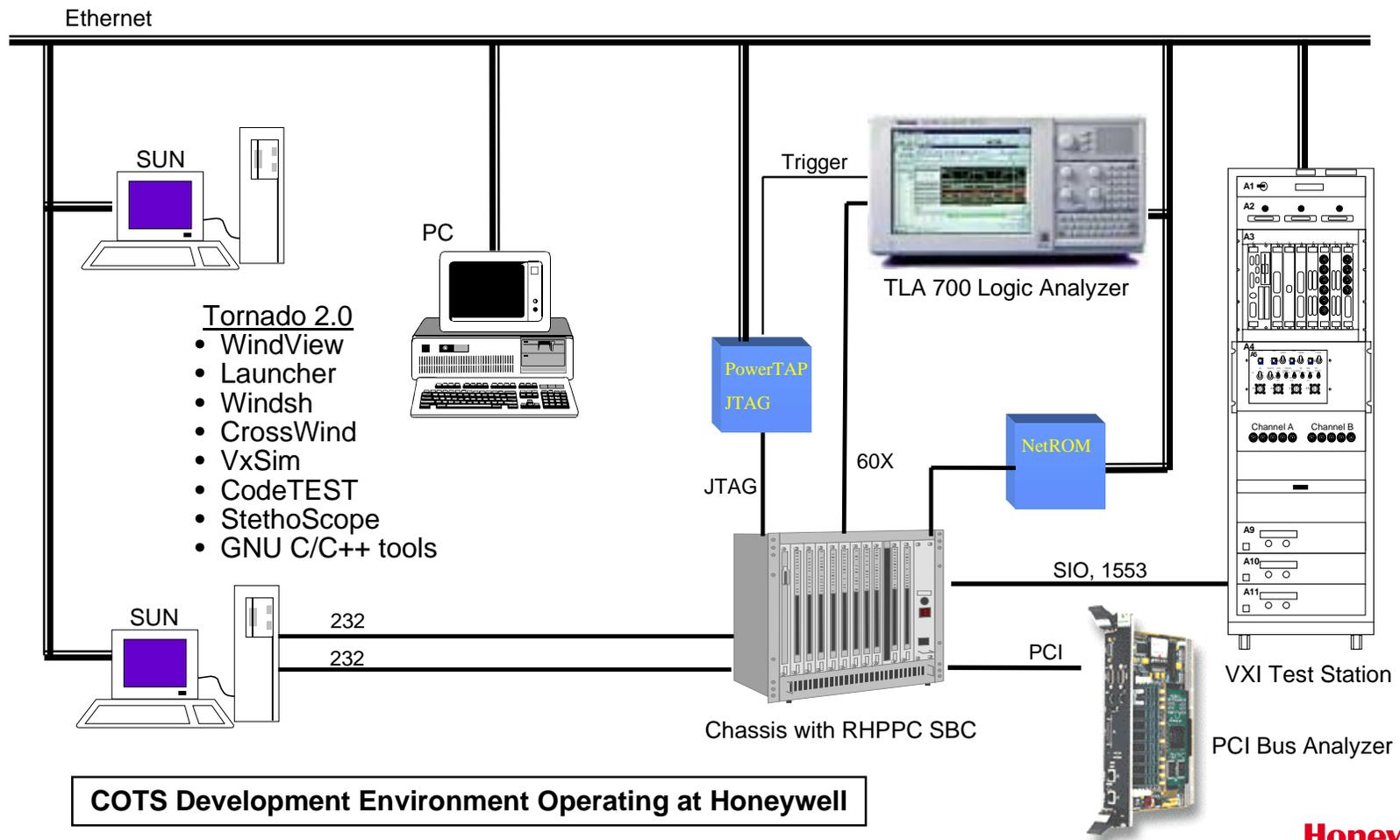
Payload Processor SBC Features

- 6U x 220mm (9.187" x 8.661"), 2.6 pounds, 12.5W (nom)
 - Two PMC-like slots (74 x 149 mm)
- 222 DMIPS @ 133 MHz RHPPC processor (cache: 32KB L1, 512KB L2)
 - PowerPC 603e™ technology licensed from Motorola
 - 33 MHz 60x bus, 64 bit data + EDAC, 32 bit address + parity
 - Power scalable with clock speed
- Memory
 - 16Mbyte SRAM, SECDED EDAC (512Kx8x4)
 - 4Mbyte EEPROM, SECDED EDAC
 - 128Kbyte PROM (SUROM)
- Backplane: cPCI, 33MHz, 32-bit, 3.3V, redundant
- I/O
 - 1553B with 8Kx16 buffer memory, transformer coupled (upgradable to dual rate 1773 with PWB mod)
 - 2 full duplex UART ports, 8250 & 16450 protocol compatible, 9.6K to 1M baud (16 bit rate register)
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Software Development Environment

- Honeywell uses the Wind River Tornado 2.0 environment
 - GNU C/C++ (gcc, gdb, xgdb)
 - PC and SUN workstations



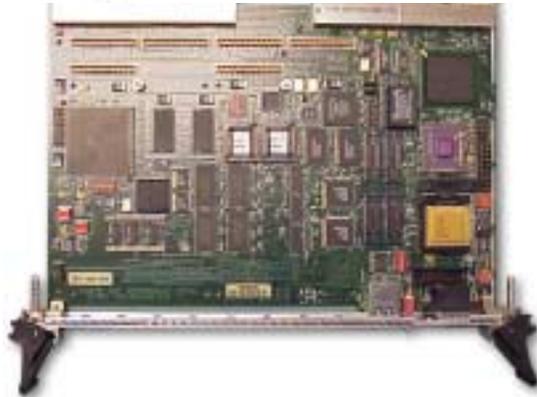
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Full Range Of Software Development Hardware



Denali from SBS Technologies

PowerPC 603e @ 200MHz
64MB SDRAM with parity
8.5MB Flash
32KB NVRAM/RTC
10Base-T/100Base-TX Ethernet
Two RS232 serial ports
PCI (MPC106)
RTOS Support from VxWorks, pSOS and HardHat Linux
6Ux160, 1 PMC slot
Available now



PDU (Ganymede) from Valley Technology Inc.

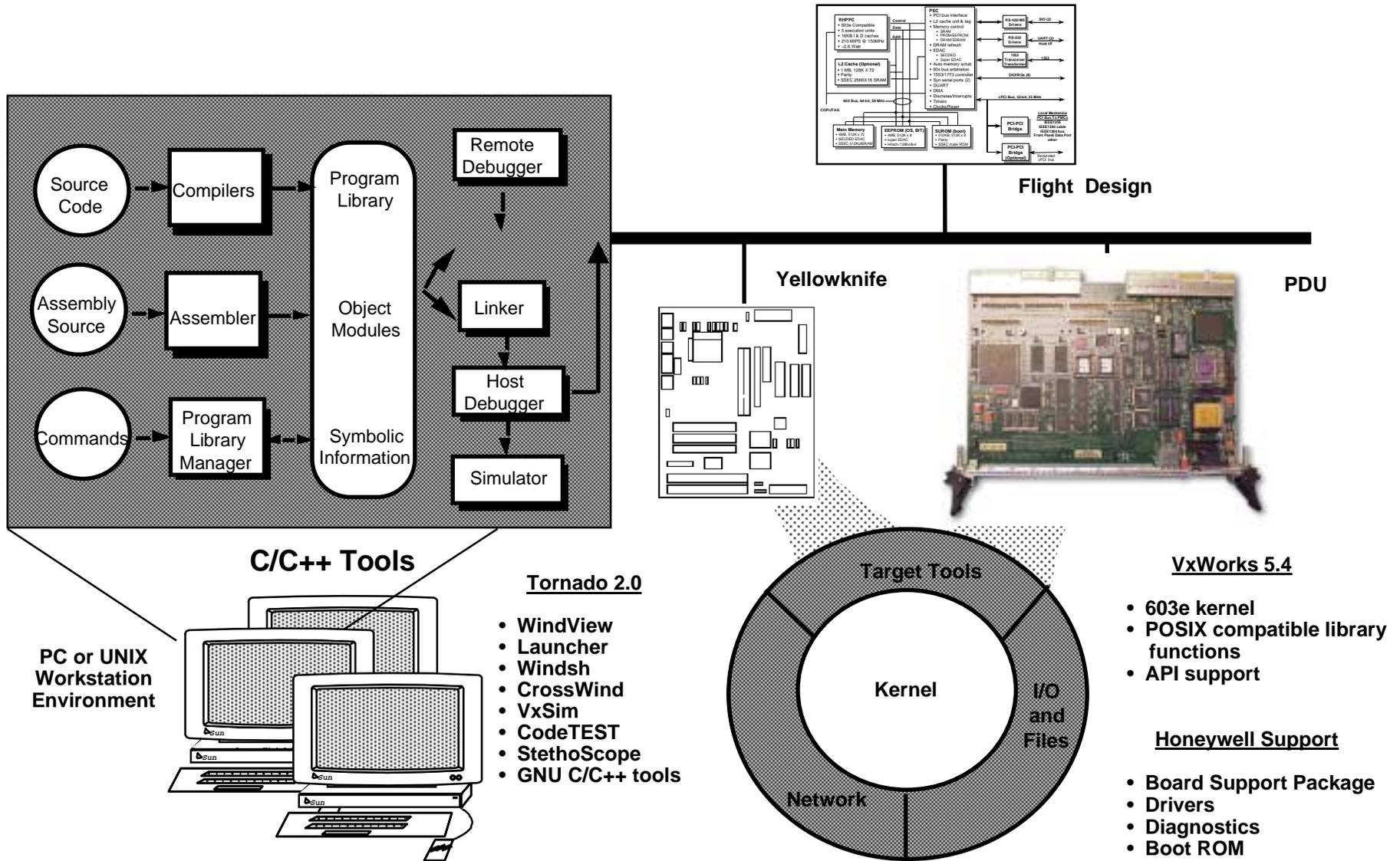
PowerPC603e or RHPPC @ 150MHz
PEC chip
1MB L2 cache
16MB SRAM or 8MB SRAM + 64MB DRAM
4MB Flash
512KB Flash (SUROM)
10Base-T/100Base-TX Ethernet
Two RS232 serial ports
PCI rev 2.2, 32-bit, 33MHz
RTOS Support from VxWorks and pSOS
6Ux160, 2 PMC slots
Available 4Q01



Calisto from Valley Technology Inc.

Same as PDU except MPC106 & 8240 replace PEC
64MB DRAM (only)
Available now

Tornado/VxWorks Summary



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Leading PowerPC™ 60x/7xx Tool Vendors

	<u>Compiler</u>	<u>Debugger</u>	<u>Emulator</u>	<u>OS</u>
Accelerated Technology				X
Applied Microsystems		X	X	
Corelis		X	X	
Cygnus Solutions	X	X		
Diab Data	X			
Enea		X		X
EST		X	X	
Green Hills Software	X	X		
Hewlett-Packard			X	
Integrated Systems Inc. (pSOS)		X		X
Lynx Real-Time Systems	X	X		X
MetaWare	X			
Metrowerks	X	X		
Mentor Graphics (Microtec)	X	X		X
Microware	X	X		X
QNX Software Systems				X
SDS		X		
Sun Microsystems (Chorus)				X
Tektronix			LA	
Wind River Systems	X	X		X

Data per Motorola SPS

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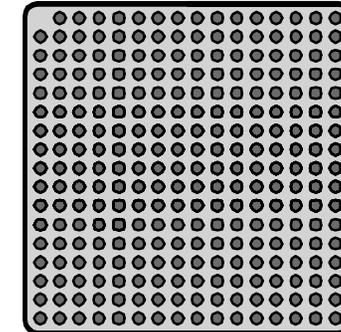
Approach

- RHPPC Processor
 - License PowerPC 603e™ technology from Motorola
 - » Best MIPS/W ratio
 - HDL (Verilog) conversion
 - » Modifications for tool differences (Type I)
 - » Modifications for hardened design style (Type II)
 - » Synthesize with hardened HX3000 library
 - » Re-implement custom blocks to be hard using SOI-V technology
 - Verify modified design using Motorola's test-bench (RTX/VCS) and verification suite (AVP), and by using Motorola's formal verification tools (MET/SLV)
 - 2 pass design
 - » 1st pass goal is full functionality and moderate (>100 MHz) performance
 - » 2nd pass goal is full 150 MHz performance
 - HX3000 standard cells, custom drop-ins, new 255 lead DBGA package
- PEC Bridge Chip
 - Design subcontracted to Boeing SSED, requirements by Honeywell
 - Re-use existing blocks modified to a common interconnect
 - ASIC verification at Boeing, system verification at Honeywell
 - HX3000 standard cells, custom drop-ins, existing 472 lead DBGA package
- Independent user assessment of features and performance
 - BSS under contract

Package Features

Common Features

- Land Grid Array
- Separates package design from board attach
 - dimple balls for test article
- 1.27 mm pitch
- Hermetic design
- 7 layers
- 1.5 mm substrate thickness
 - Includes 0.2mm dimple layer
- 1.2 mm hermetic lid thickness
- Al wirebond die interconnect
- Alumina construction
 - 90% Al₂O₃, Er=9.8



Features Unique to RHPPC

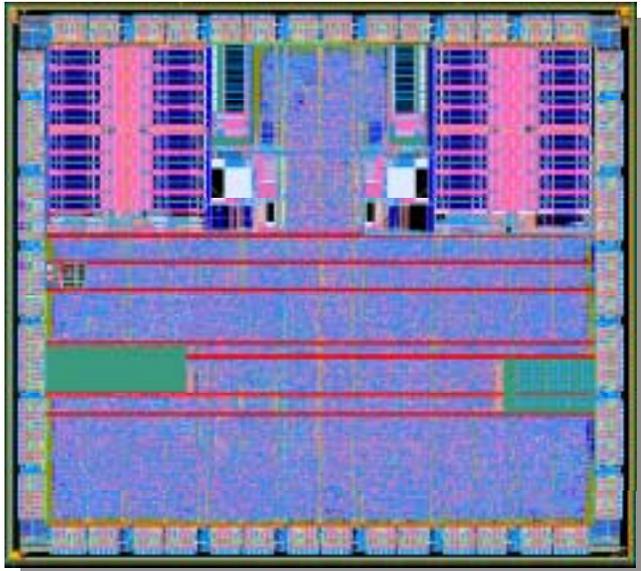
- 255 land grid array (16 x 16)
- Footprint compatible with commercial PPC BGA
- 21 X 21 mm (same as commercial part)
- 7 grams approx.
- 2.6W (typ), 3.5W (peak)

Features Unique to PEC

- 472 land grid array (22 x 22)
- 29 X 29 mm
- 9 grams approx.
- 2.5W (typ), 3.5W (peak)

LGA Design Separates Board Attach Concerns from Package Design

RHPPC Processor Overview



Technology

- 0.35 μ m, 4 level metal, SOI-V
- HX3000 standard cell with custom drop-ins
- Single chip with CPU, FPU, Cache
- Rad Hard for military space applications

TD	>5E5	Rad(Si)
DRU	>1E9	Rad(Si)/s
DRS	>1E11	Rad(Si)/s
SEU	<4.8E-5	Upset/Chip-Day
Will not latch up		

- Package: 255 lead grid array
 - 21 x 21 mm, 1.27 mm pitch
- Testability coverage > 99%

Features

- Compatible with commercial PowerPC 603e™
 - Architecture (books 1 - 3)
 - Programmer's interface
 - Boolean equivalent except for PLL & PVR
 - Footprint compatible
- 222 MIPS (Dhrystone) @ 133MHz (1.67 IPC)
 - 25 to 150 MHz core frequencies supported
- 25, 33.3, 40 or 50 MHz 60x bus
- 3.3V core & I/O
- 2.6W (nom), 3.5W (WC) - 81 MIPS/Watt
- Icache/Dcache 16Kbyte each
- IEEE 754 floating point
- Supports multiprocessing (Cache Snooping)
- Power management (dynamic, doze, nap, sleep)
- QML Q+ procurable (class S equivalent)

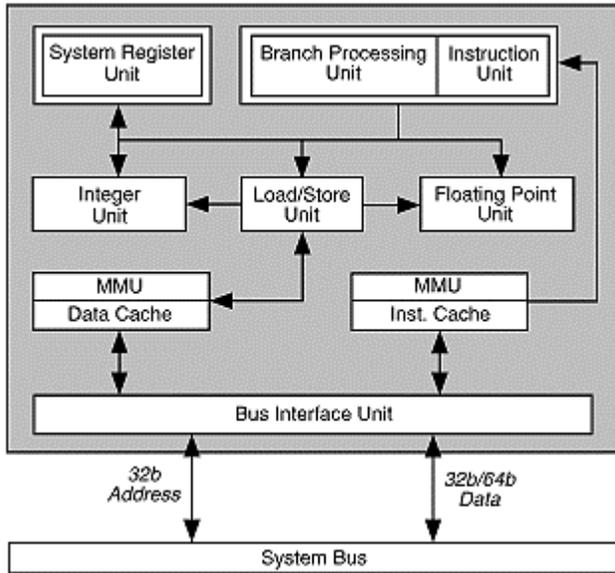
Application Support

- All commercial PowerPC 603e™ tools and OS
 - C/C++ & Ada 95 tools
 - VxWorks real time OS
- Prototype Development Unit (PDU) for quick prototyping and hardware/software integration ahead of flight hardware

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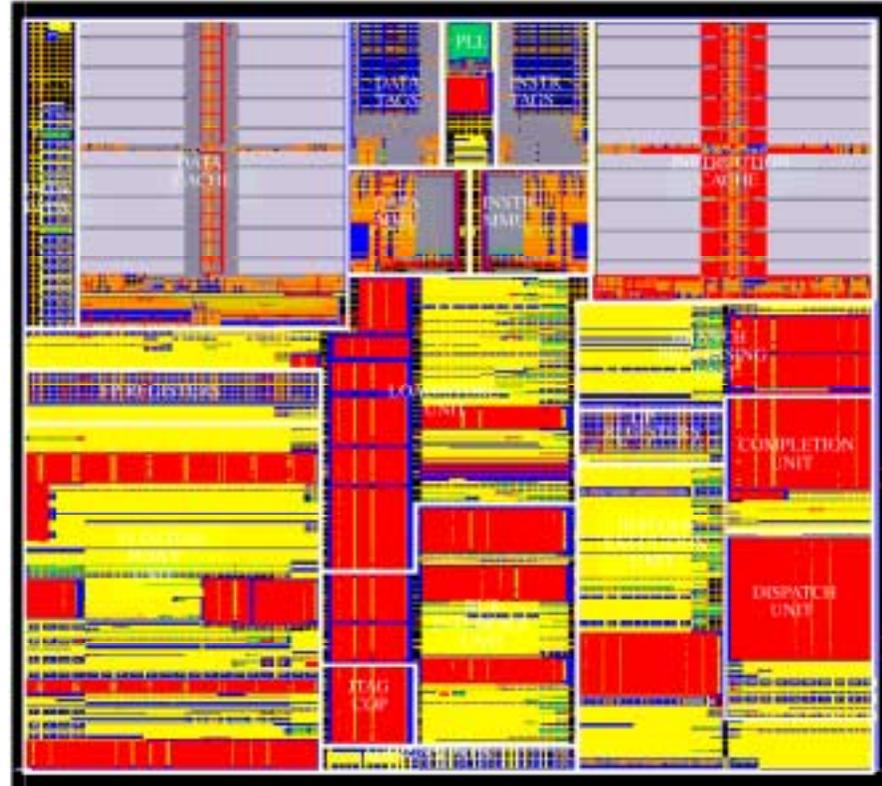
Motorola PowerPC 603e™ G2/Groucho Core

PowerPC 603e™ Microprocessor Block Diagram



Embeddable core version (G2)
 2.6M Transistors
 34mm²
 0.28μm, 5 LM
 1.5W (nom) @ 150 MHz (no I/O)
 2.5V operation
 Testability > 99%

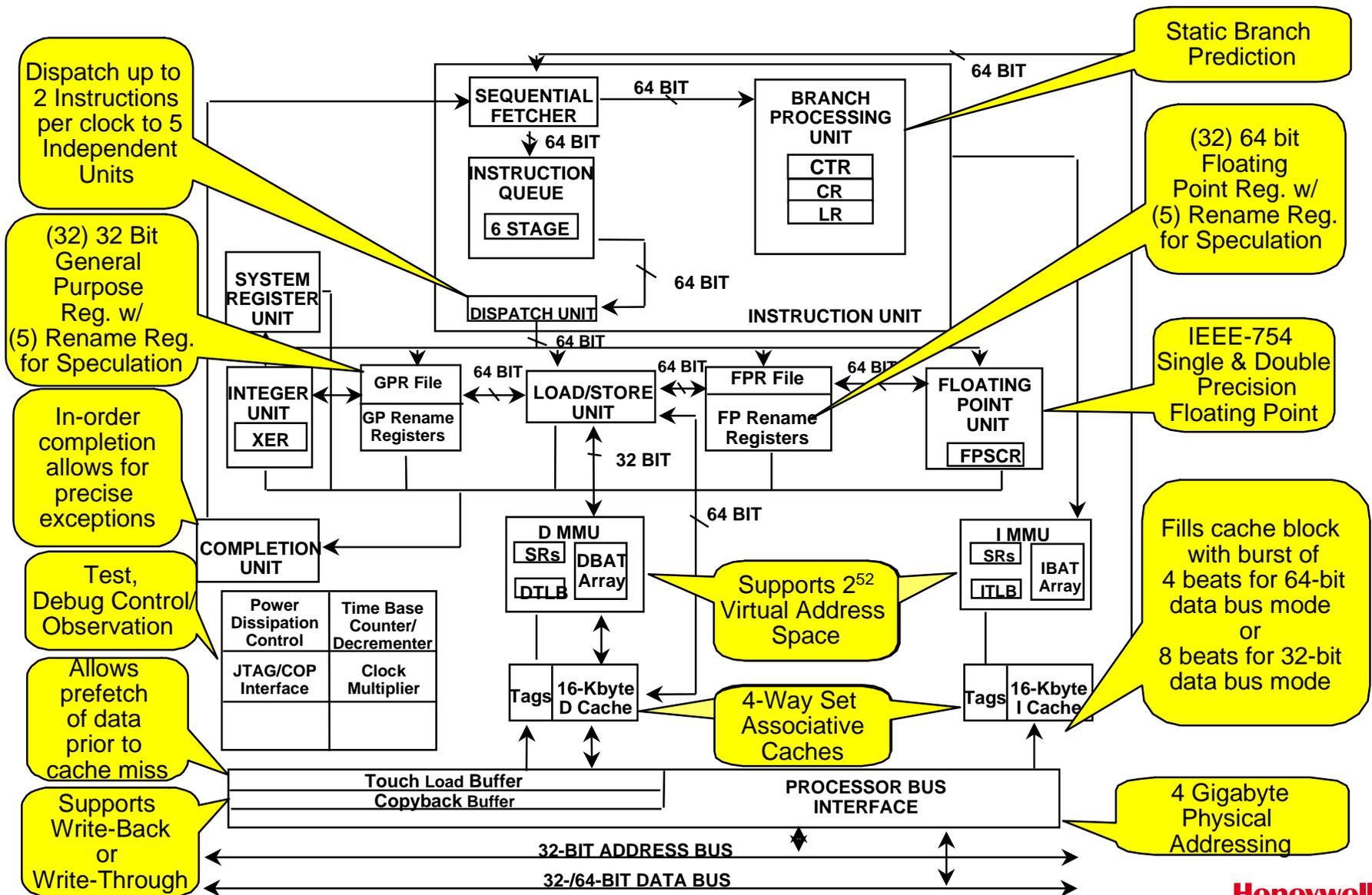
PowerPC 603e™ Microprocessor Layout



Data path (OTS), Control (RLM), Custom, Analog

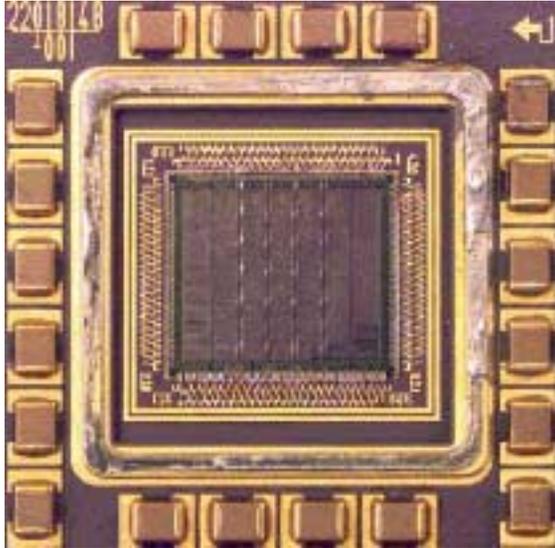
Commercial core being used in many new designs and continues to be upgraded by Motorola.

RHPPC Processor Block Diagram



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PEC Overview



Technology

- 0.35 μ m, 4 level metal, SOI-V
- HX3000 standard cell with custom drop-ins
- Rad Hard for military space applications

TD	>5E5	Rad(Si)
DRU	>1E9	Rad(Si)/s
DRS	>1E11	Rad(Si)/s
SEU (w/o L2)	<1E-7	Upset/Chip-Day
SEU (w L2)	<6E-5	Upset/Chip-Day
Will not latch up		

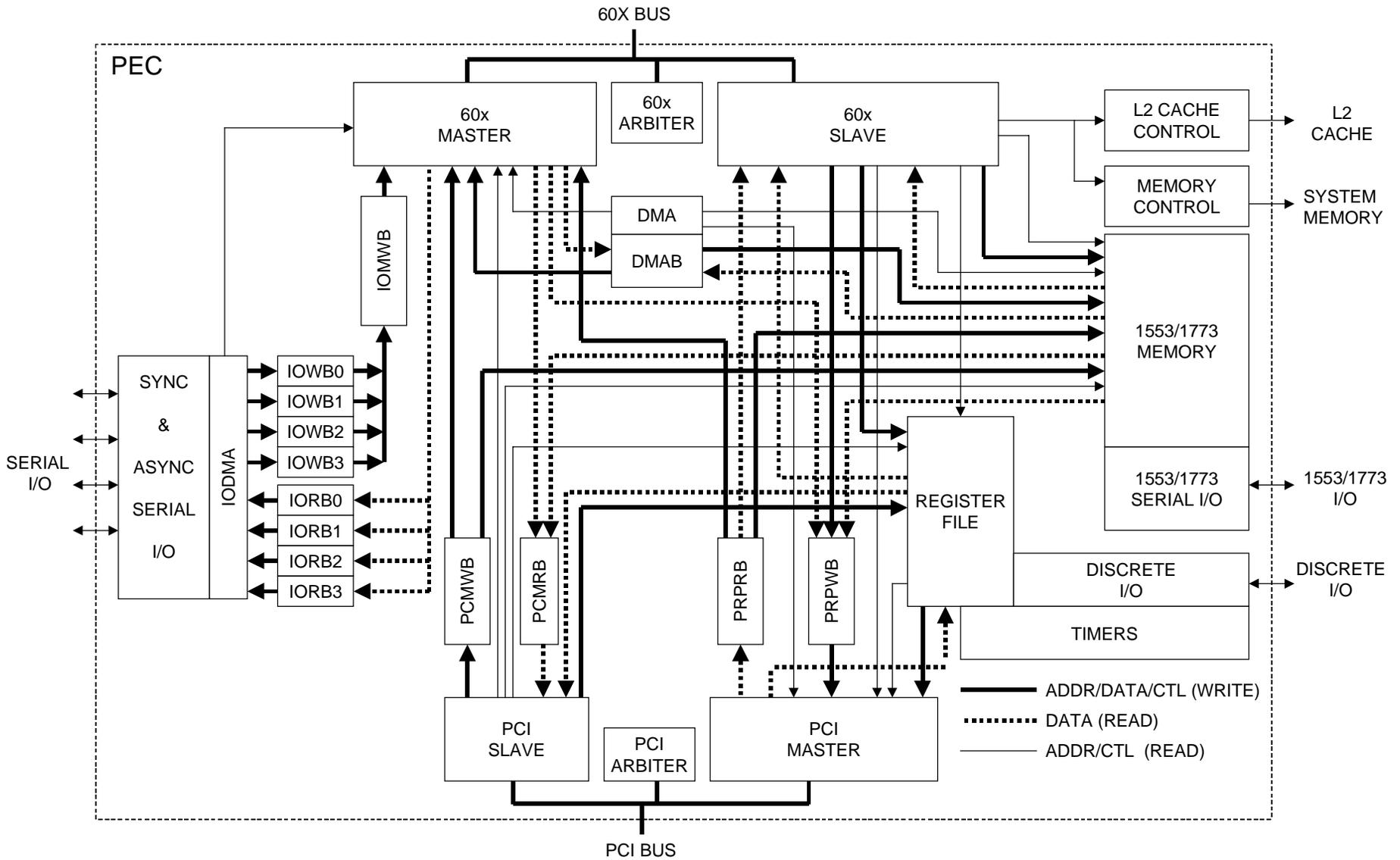
- Package: 472 lead grid array
 - 29 x 29 mm, 1.27 mm pitch
- Testability coverage > 95%

Features

- 25, 33.3, 40, 50 & 66 MHz, 64-bit 60x bus
- 512KB level 2 cache controller
 - On-chip tag RAM, 1 GB cachable space
 - Direct mapped, write through
- Configurable memory controller interfaces to PROM, EEPROM, SRAM, and DRAM
 - Contiguous memory space
 - DRAM refresh controller
 - Parity, SECCDED EDAC, super EDAC
 - Auto memory scrub
 - Address map B (CHRP)
- Generates resets & clocks for RHPPC
- 4 General Purpose, Mission, and Two Stage Watchdog Timers
- 16.7, 20, 25 or 33 MHz, 32 bit PCI bus (rev 2.2)
- 1553/1773 protocol controller, internal data buffer
- 2 full duplex programmable synchronous serial ports
 - Baud rate fourth or fortieth SYSCLK (1.25/12.5 Mbps @ 50MHz)
 - Data/Clock/Sync, odd parity
- 2 full duplex 8250 compatible serial UART ports
 - 16-bit rate register (9600 to 1M baud @ 50MHz)
 - Programmable
- 16 programmable interrupts or discretives
- 2 DMA Controllers: 1 for I/O, 1 for memory/PCI
- Software compatible with MPC106 Bridge Chip
 - Implemented functions will remain compatible
- 3.3V, 2.5 W nom, 3.5 W max
 - Supports power management
- QML Q+ procurable (Class S equivalent)

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PEC Block Diagram



Status

- Payload Controller SBC design underway, EM unit 1Q02.
- RHPPC pass 1 first silicon delivered to Clearwater 12/22/00.
 - Full functionality and compatibility with commercial part proven
 - » YellowKnife and Calisto boards, pSOS and VxWorks RTOS
 - Operates at 100MHz.
 - Quick look radiation testing completed
 - » TID >1E6
 - » DRU >2E10
 - » SEU 2.4E-4 (expected due to know problems with storage elements)
- PHPPC pass 2 is underway. Using new PKS tool.
 - Expect 133MHz operation
 - Expect first silicon before year-end
- PEC has struggled but is under control.
 - PDR 2/22/01
 - CDR/tapeout 9/01
 - POD 12/01

RHPPC SBC Benefits

- True commercial compatibility, open architecture
 - PowerPC603e™ technology licensed from Motorola
 - » Many mature and supported software development tools available
 - » Motorola & IBM plan to support this instruction set for many years
 - VxWorks RTOS
 - cPCI & PMC form factor, cPCI backplane, PCI mezzanine bus
 - MIL-STD-1553, RS422, RS232 I/O
- High performance
 - 222 DMIPS @ 11W => 20.2 MIPS/W at board level
 - Enables payload functions not possible before
- True space level radiation hardness
- Simple architecture results in:
 - High reliability
 - Low power
 - Low cost

RHPPC processor chips are functional